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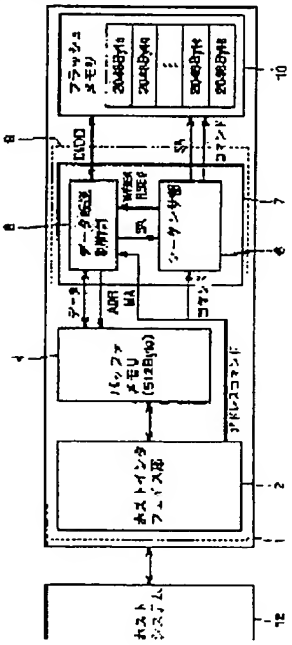
(71)Applicant : MITSUBISHI ELECTRIC CORP
(72)Inventor : FUKUZUMI TOMOYA

(54) STORAGE MEDIUM ON WHICH FLASH MEMORY IS MOUNTED

(57)Abstract:
PROBLEM TO BE SOLVED: To obtain a low-cost storage device capable of using a buffer memory having capacity being smaller than the sector capacity of a mounted flash memory.
SOLUTION: This storage device 1 uses two bits in a low order of a media sector address received from a host system 12 as data corresponding to a column address in a sector of a flash memory 10. A data transfer controlling part 8 starts data transfer to the memory 10 from a buffer memory 4 in timing corresponding to column addresses 0h, 200h, 400h and 600h respectively, for instance, on the case low order two bits 00, 01, 10 and 11 of a media sector address are inputted when the sector capacity of the memory 10 is defined as 2048 bytes and the sector capacity of the device 1 is defined as 512 bytes.



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(71)出願人　000006013
三菱電機株式会社
東京都千代田区丸の内二丁目２番３号
(72)発明者　福住　知也
東京都千代田区丸の内二丁目２番３号　三菱電機株式会社内
(74)代理人　100064746
弁理士　深見　久郎　（外３名）

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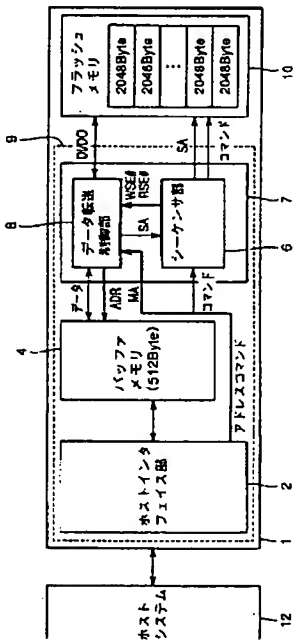
(54)【発明の名称】　フラッシュメモリを搭載する記憶装置

(57)【要約】
【課題】　搭載するフラッシュメモリのセクタ容量より小容量のバッファメモリを使用することを可能にした、低コストの記憶装置を提供することである。
【解決手段】　記憶装置がホストシステムより受けるメディアセクタアドレスの下位２ビットを、フラッシュメモリのセクタ内のカラムアドレスに対応するデータとして使用する。例えば、フラッシュメモリのセクタ容量が２０４８バイトで記憶装置のセクタ容量が５１２バイトである場合において、データ転送制御部８はメディアセクタアドレスの下位２ビットＣ０、０１、１０，１１が入力されるとそれぞれカラムアドレス０ｈ、２００ｈ、４００ｈ、６００ｈに対応するタイミングでバッファメモリからフラッシュメモリへのデータ転送を開始する。



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【特許請求の範囲】

【請求項１】　ホストシステムから外部書込アドレス信号と外部書込データとを受けてデータ記憶を行う書込モードを備える記憶装置であって、

データ消去時には所定数のデータを保持するメモリ領域を最小単位とする一括消去が行われ　前記所定数のデータ長を単位として複数のデータの書込がなされるフラッシュメモリを備え、

前記フラッシュメモリは、前記書込モードにおいて、内部書込アドレス信号を受けて、内部書込データに含まれる複数のデータを取込み保持し、

前記書込モードにおいて、前記外部書込アドレス信号を受けて前記内部書込アドレス信号を発生し、前記外部書込データを受けて保持して前記外部書込データと前記外部書込アドレス信号とに基づいて前記内部書込データを出力するデータ入出力部をさらに備え、

前記データ入出力部は、

前記書込モードにおいて、前記ホストシステムから前記外部書込データおよび前記外部書込アドレス信号を受ける第１のインタフェイス部と、

前記外部書込データの数以上で、かつ、前記内部書込データの数より少ない記憶容量を有し、前記書込モードにおいて前記第１のインタフェイス部から前記外部書込データを受け取る、バッファメモリと、

前記書込モードにおいて、前記第１のインタフェイス部から前記外部書込アドレス信号を受けて前記内部書込アドレス信号を発生し、前記バッファメモリから読出した前記外部書込データに前記メモリ領域のデータ書換が生じない前記外部書込アドレス信号に対応するダミーデータを加えて前記内部書込データを発生する第２のインタフェイス部とを含む、フラッシュメモリを搭載する記憶装置。

【請求項２】　前記ダミーデータは、前記フラッシュメモリがデータ消去された直後に保持するデータに対応する値であり、

前記第２のインタフェイス部は、前記内部書込データに含まれる前記データ長のデータを所定の順序で逐次出力し、

前記外部書込データは、前記所定の順序において前記外部書込アドレス信号に対応する位置を先頭位置とする連続する位置を占める、請求項１に記載のフラッシュメモリを搭載する記憶装置。

【請求項３】　前記先頭位置は、前記外部書込アドレス信号に応じて前記外部書込データに含まれるデータ数を単位として前記所定の順序の第１番目を基準にして不連続に決定される、請求項２に記載のフラッシュメモリを搭載する記憶装置。

【請求項４】　前記内部書込データに含まれるデータ数は、前記外部書込データに含まれるデータ数の整数倍である、請求項３に記載のフラッシュメモリを搭載する記憶装置。

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【請求項５】　前記フラッシュメモリは、クロックに同期して前記内部書込データを順次取込み、

前記第２のインタフェイス部は、

前記バッファメモリに対する読出制御信号を発生して前記バッファメモリから前記外部書込データを受けて前記内部書込データを発生し、前記外部書込アドレス信号から前記内部書込アドレス信号を発生する、データ転送制御部を有し、

前記データ転送制御部は、

前記フラッシュメモリに前記内部書込データの書込が開始されるときに、前記クロックのカウントを開始するカウンタと、

前記外部書込アドレス信号に含まれるオフセット信号と前記カウンタのカウント値の上位から所定数ビットとが一致した時に一致信号を出力する比較器と、

前記バッファメモリが前記クロックに同期して前記外部書込データを出力するように前記一致信号に応じて読出制御信号を前記バッファメモリに与えるゲート回路と、

前記一致信号が非活性化されている時は前記フラッシュメモリの消去後の初期値に対応する値を前記フラッシュメモリに与え、前記一致信号が活性化した時は前記バッファメモリから読出された前記外部書込データを前記フラッシュメモリに与える選択回路とを有する、請求項２に記載のフラッシュメモリを搭載する記憶装置。

【請求項６】　前記記憶装置は、前記ホストシステムから外部読出アドレス信号を受けて前記ホストシステムに外部読出データを出力する読出モードをさらに備え、

前記データ入出力部は、前記読出モード時に、前記外部読出アドレス信号を受けて内部読出アドレス信号を発生して前記フラッシュメモリに与え、前記フラッシュメモリから読出される内部読出データの一部を選択して前記外部読出データとして保持した後、前記ホストシステムに対して前記外部読出データを出力し、

前記第１のインタフェイス部は、前記読出モード時に、前記ホストシステムから受けた前記外部読出アドレス信号に応じた前記外部読出データを前記ホストシステムに出力し、

前記バッファメモリは、前記外部読出データの数以上で、かつ、前記内部読出データの数より少ない記憶容量を有し、前記読出モード時に、前記第１のインタフェイス部に対して保持していた前記外部読出データを出力し、

前記第２のインタフェイス部は、前記読出モード時に、前記第１のインタフェイス部から前記外部読出アドレス信号を受けて前記内部読出アドレス信号を発生して前記フラッシュメモリに与えて前記フラッシュメモリから前記内部読出データが含む複数のデータを読出し、前記内部読出しデータの一部を前記外部読出データとしてバッファメモリに送出する、請求項１に記載のフラッシュメ

モリを搭載する記憶装置。

【請求項７】　前記フラッシュメモリは、前記内部読出アドレス信号に応じて前記内部読出データに含まれる前記データ長のデータを所定の順序で逐次出力し、

前記外部読出データは、前記所定の順序において前記外部読出アドレス信号に対応する位置を先頭位置とする連続する位置を占める、請求項６に記載のフラッシュメモリを搭載する記憶装置。

【請求項８】　前記先頭位置は、前記外部読出アドレス信号に応じて前記外部読出データに含まれるデータ数を単位として前記所定の順序の第１番目を基準にして不連続に決定される、請求項７に記載のフラッシュメモリを搭載する記憶装置。

【請求項９】　前記内部書込データに含まれるデータ数は、前記外部書込データに含まれるデータ数の整数倍である、請求項８に記載のフラッシュメモリを搭載する記憶装置。

【請求項１０】　前記フラッシュメモリは、クロックに同期して前記内部読出データを順次出力し、

前記第２のインタフェイス部は、

前記外部読出アドレス信号から前記内部読出アドレス信号を発生し、前記内部読出データの一部を選択して前記外部読出データとして前記バッファメモリが格納するようにバッファメモリへ書込制御信号を発生する、データ転送制御部を有し、

前記データ転送制御部は、

前記フラッシュメモリから前記内部読出データの読出が開始されるときに、前記クロックのカウントを開始するカウンタと、

前記外部書込アドレス信号に含まれるオフセット信号と前記カウンタのカウント値の上位から所定数ビットとが一致した時に一致信号を出力する比較器と、

前記バッファメモリが前記クロックに同期して前記内部読出データの一部を前記外部読出データとして格納するように前記一致信号に応じて前記書込制御信号を前記バッファメモリに与えるゲート回路とを有する、請求項７に記載のフラッシュメモリを搭載する記憶装置。

【請求項１１】　ホストシステムから外部アドレス信号を受けて外部データを授受するデータ記憶を行う記憶装置であって、

前記外部アドレスに対応する内部主アドレスおよび内部副アドレスを発生するデータ入出力部と、

データ消去時には所定数のデータを保持するメモリ領域を最小単位とする一括消去が行われ、前記内部主アドレスによって前記メモリ領域単位の選択が行われ、前記内部副アドレスによって前記メモリ領域内のデータ授受開始位置が指定され複数のデータを含む内部データを逐次授受することが可能なフラッシュメモリとを備え、

前記メモリ領域の記憶容量は、前記外部データに含まれるデータ数より大きく、

前記内部副アドレスは、前記外部書込データに含まれるデータ数を単位として前記メモリ領域の先頭アドレスを基準として不連続に発生される、フラッシュメモリを搭載する記憶装置。

【請求項１２】　前記データ入出力部は、

前記ホストシステムと前記フラッシュメモリとの間のタイミング調整をするために前記外部データと前記内部データとを一時的に保持する前記外部データに含まれるデータ数に対応する記憶容量を有するバッファメモリを含む、請求項１１に記載のフラッシュメモリを搭載する記憶装置。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は、記憶装置に関し、より特定的には、フラッシュメモリを搭載する記憶装置に関する。

【０００２】

【従来の技術】近年、半導体製造技術の進歩に伴い、フラッシュメモリの記憶容量も大きくなってきている。この大容量化に伴い、小型でかつ低消費電力である特性を生かして特に携帯機器の分野においては記録メディアとしてフラッシュメモリを搭載した記憶装置が使用されるようになってきた。

【０００３】

【発明が解決しようとする課題】フラッシュメモリは、不揮発性で、一括消去後再書込ができる半導体記憶装置である。フラッシュメモリは、高密度に記憶素子を集積し、かつ、高速にデータ授受をするため、セクタアドレスを指定して一定量のデータをセクタ単位で読出、消去、書込（プログラム）を一括して行う。フラッシュメモリの大容量化に伴い、フラッシュメモリが一括してデータを読出す単位であるセクタ容量も増加する傾向にあり、たとえば、２５６MビットのＡＮＤ型フラッシュメモリではこのセクタ容量は２０４８バイトになっている。

【０００４】一方、パーソナルコンピュータを初めとする情報機器がハードディスクやメモリカード等の記憶装置とデータ授受を行なう際の単位のデータ容量（本明細書中では以降メディアセクタ容量と称する）は、たとえば、標準的には５１２バイトであり、このメディアセクタ容量は特に増加する傾向は見られない。

【０００５】このような、セクタ構造を持ったフラッシュメモリを搭載する記憶装置では、フラッシュメモリのセクタデータを一時的に格納し、ホストシステムとのデータ転送を行なうためのタイミングおよび容量の調整を行なうためのバッファメモリを記憶装置の内部に搭載する必要がある。このバッファメモリは通常ＳＲＡＭ（Static Random Access Memory）等が用いられる。

【０００６】ホストシステムとのデータ転送の容量、すなわちメディアセクタ容量が、フラッシュメモリのセク

タ容量よりも小容量である場合でも、バッファメモリの容量は、フラッシュメモリのセクタ容量と同容量もしくはそれ以上の容量にする必要があった。

【０００７】しかしながら、フラッシュメモリのセクタ容量が年々大容量化しつつあり、このような場合には、バッファメモリとして大容量のＳＲＡＭを搭載する必要があり、コスト的にデメリットが生じていた。

【０００８】本発明は、このような問題点を解決するようになされたもので、その目的は、メディアセクタ容量に相当する小容量のバッファメモリを搭載することを可能にし、コストダウンを図ったフラッシュメモリを搭載する記憶装置を提供することである。

【０００９】

【課題を解決するための手段】請求項１に記載のフラッシュメモリを搭載する記憶装置は、ホストシステムから外部書込アドレス信号と外部書込データとを受けてデータ記憶を行う書込モードを備える記憶装置であって　データ消去時には所定数のデータを保持するメモリ領域を最小単位とする一括消去が行われ、所定数のデータ長を単位として複数のデータの書込がなされるフラッシュメモリを備え、フラッシュメモリは、書込モードにおいて、内部書込アドレス信号を受けて、内部書込データに含まれる複数のデータを取込み保持し、書込モードにおいて、外部書込アドレス信号を受けて内部書込アドレス信号を発生し、外部書込データを受けて保持して外部書込データと外部書込アドレス信号とに基づいて内部書込データを出力するデータ入出力部をさらに備え、データ入出力部は、書込モードにおいて、ホストシステムから外部書込データおよび外部書込アドレス信号を受ける第１のインタフェイス部と、外部書込データの数以上で、かつ、内部書込データの数より少ない記憶容量を有し、書込モードにおいて第１のインタフェイス部から外部書込データを受け取る、バッファメモリと、書込モードにおいて、第１のインタフェイス部から外部書込アドレス信号を受けて内部書込アドレス信号を発生し、バッファメモリから読出した外部書込データにメモリ領域のデータ書換が生じない外部書込アドレス信号に対応するダミーデータを加えて内部書込データを発生する第２のインタフェイス部とを含む。

【００１０】請求項２に記載のフラッシュメモリを搭載する記憶装置は、請求項１に記載のフラッシュメモリを搭載する記憶装置の構成において、ダミーデータは、フラッシュメモリがデータ消去された直後に保持するデータに対応する値であり、第２のインタフェイス部は、内部書込データに含まれるデータ長のデータを所定の順序で逐次出力し、外部書込データは、所定の順序において外部書込アドレス信号に対応する位置を先頭位置とする連続する位置を占める。

【００１１】請求項３に記載のフラッシュメモリを搭載する記憶装置は、先頭位置は、請求項２に記載のフラッシュメモリを搭載する記憶装置の構成において、外部書込アドレス信号に応じて外部書込データに含まれるデータ数を単位として所定の順序の第１番目を基準にして不連続に決定される。

【００１２】請求項４に記載のフラッシュメモリを搭載する記憶装置は、請求項３に記載のフラッシュメモリを搭載する記憶装置の構成において、内部書込データに含まれるデータ数は、外部書込データに含まれるデータ数の整数倍である。

【００１３】請求項５に記載のフラッシュメモリを搭載する記憶装置は、請求項２に記載のフラッシュメモリを搭載する記憶装置の構成に加えて、フラッシュメモリは、クロックに同期して内部書込データを順次取込み、第２のインタフェイス部は、バッファメモリに対する読出制御信号を発生してバッファメモリから外部書込データを受けて内部書込データを発生し、外部書込アドレス信号から内部書込アドレス信号を発生する、データ転送制御部を有し、データ転送制御部は、フラッシュメモリに内部書込データの書込が開始されるときに、クロックのカウントを開始するカウンタと、外部書込アドレス信号に含まれるオフセット信号とカウンタのカウント値の上位から所定数ビットとが一致した時に一致信号を出力する比較器と、バッファメモリがクロックに同期して外部書込データを出力するように一致信号に応じて読出制御信号をバッファメモリに与えるゲート回路と、一致信号が非活性化されている時はフラッシュメモリの消去後の初期値に対応する値をフラッシュメモリに与え、一致信号が活性化した時はバッファメモリから読出された外部書込データをフラッシュメモリに与える選択回路とを有する。

【００１４】請求項６に記載のフラッシュメモリを搭載する記憶装置は、請求項１に記載のフラッシュメモリを搭載する記憶装置の構成に加えて、ホストシステムから外部読出アドレス信号を受けてホストシステムに外部読出データを出力する読出モードをさらに備え、データ入出力部は、読出モード時に、外部読出アドレス信号を受けて内部読出アドレス信号を発生してフラッシュメモリに与え、フラッシュメモリから読出される内部読出データの一部を選択して外部読出データとして保持した後、ホストシステムに対して外部読出データを出力し、第１のインタフェイス部は、読出モード時に、ホストシステムから受けた外部読出アドレス信号に応じた外部読出データをホストシステムに出力し、バッファメモリは、外部読出データの数以上で、かつ、内部読出データの数より少ない記憶容量を有し、読出モード時に、第１のインタフェイス部に対して保持していた外部読出データを出力し、第２のインタフェイス部は、読出モード時に、第１のインタフェイス部から外部読出アドレス信号を受けて内部読出アドレス信号を発生してフラッシュメモリに与えてフラッシュメモリから内部読出データが含む複数

のデータを読出し、内部読出しデータの一部を外部読出データとしてバッファメモリに送出する。

【００１５】請求項７に記載のフラッシュメモリを搭載する記憶装置は、請求項６に記載のフラッシュメモリを搭載する記憶装置の構成に加えて、フラッシュメモリは、内部読出アドレス信号に応じて内部読出データに含まれるデータ長のデータを所定の順序で逐次出力し、外部読出データは、所定の順序において外部読出アドレス信号に対応する位置を先頭位置とする連続する位置を占める。

【００１６】請求項８に記載のフラッシュメモリを搭載する記憶装置は、請求項７に記載のフラッシュメモリを搭載する記憶装置の構成において、先頭位置は、外部読出アドレス信号に応じて外部読出データに含まれるデータ数を単位として所定の順序の第１番目を基準にして不連続に決定される。

【００１７】請求項９に記載のフラッシュメモリを搭載する記憶装置は、請求項８に記載のフラッシュメモリを搭載する記憶装置の構成において、内部書込データに含まれるデータ数は、外部書込データに含まれるデータ数の整数倍である。

【００１８】請求項１０に記載のフラッシュメモリを搭載する記憶装置は、請求項７に記載のフラッシュメモリを搭載する記憶装置の構成に加えて　フラッシュメモリは、クロックに同期して内部読出データを順次出力し、第２のインタフェイス部は、外部読出アドレス信号から内部読出アドレス信号を発生し、内部読出データの一部を選択して外部読出データとしてバッファメモリが格納するようにバッファメモリへ書込制御信号を発生する、データ転送制御部を有し、データ転送制御部は、フラッシュメモリから内部読出データの読出が開始されるときに、クロックのカウントを開始するカウンタと、外部書込アドレス信号に含まれるオフセット信号とカウンタのカウント値の上位から所定数ビットとが一致した時に一致信号を出力する比較器と、バッファメモリがクロックに同期して内部読出データの一部を外部読出データとして格納するように一致信号に応じて書込制御信号をバッファメモリに与えるゲート回路とを有する。

【００１９】請求項１１に記載のフラッシュメモリを搭載する記憶装置は、ホストシステムから外部アドレス信号を受けて外部データを授受するデータ記憶を行う記憶装置であって、外部アドレスに対応する内部主アドレスおよび内部副アドレスを発生するデータ入出力部と、データ消去時には所定数のデータを保持するメモリ領域を最小単位とする一括消去が行われ、内部主アドレスによってメモリ領域単位の選択が行われ、内部副アドレスによってメモリ領域内のデータ授受開始位置が指定され複数のデータを含む内部データを逐次授受することが可能なフラッシュメモリとを備え、メモリ領域の記憶容量は、外部データに含まれるデータ数より大きく、内部副アドレスは、外部書込データに含まれるデータ数を単位としてメモリ領域の先頭アドレスを基準として不連続に発生される。

【００２０】請求項１２に記載のフラッシュメモリを搭載する記憶装置は、請求項１１に記載のフラッシュメモリを搭載する記憶装置の構成に加えて、データ入出力部は、ホストシステムとフラッシュメモリとの間のタイミング調整をするために外部データと内部データとを一時的に保持する外部データに含まれるデータ数に対応する記憶容量を有するバッファメモリを含む。

【００２１】

【発明の実施の形態】以下図面を参照しつつ、本発明の実施の形態について詳しく説明する。なお、図中同一符号は、同一または相当部分を示す。

【００２２】［実施の形態１］図１は、フラッシュメモリを搭載した記憶装置１の概略構成を示すブロック図である。

【００２３】図１を参照して、記憶装置１は、ホストシステム１２と記憶する外部データの授受を行なうためのものであり、ホストシステムからメディアアドレスを受けてアドレス変換を行い、ホストシステムの間で外部データを授受するためにデータ変換を行うデータ入出力部９と、データ入出力部９が変換したアドレス信号に応じてデータ授受を行うフラッシュメモリ１０とを含む。データ入出力部９はフラッシュメモリ１０が入出力するデータと外部データとの間のデータの変換を行う。

【００２４】データ入出力部９は、ホストシステムとデータ転送を行なうホストインタフェイス部２と、ホストインタフェイス部２がホストシステム１２とデータ転送を行なうためにフラッシュメモリのセクタデータの一部を一時的に格納する５１２バイトの容量を持つバッファメモリ４と、ホストインタフェイス部２からの指令に応じてバッファメモリ４とフラッシュメモリとのデータ授受のコントロールを行なうフラッシュインタフェイス部７と、記憶装置１が記憶すべきデータを保持する半導体装置であるフラッシュメモリ１０とを含む。

【００２５】フラッシュインタフェイス部７は、フラッシュメモリの仕様にあわせたシーケンスで、読出や書込等の動作を設定するコマンドや、読出や書込時にメモリ領域を指定するためのアドレスをフラッシュメモリに送出するシーケンサ部６と、ホストシステム１２から与えられたメディアセクタアドレスからフラッシュメモリのセクタアドレスおよびカラムアドレスオフセットを生成するデータ転送制御部８とを含む。

【００２６】フラッシュメモリ１０は、各々が２０４８バイトの容量を持つ複数のセクタを有する。フラッシュメモリ１０は、セクタアドレスが指定されると、指定されたセクタに記憶されている２０４８バイトのデータをシリアルに出力することができる。

【００２７】図２は、実施の形態１におけるフラッシュ

メモリとバッファメモリとのアドレスの対応関係を示すメモリマップである。

【００２８】図２を参照して、メディアセクタ容量、すなわち記憶装置１が一括してデータ授受を行なうセクタ容量が５１２バイト、フラッシュメモリ１０の１セクタが５４８バイトである場合のメモリアップであり、フラッシュメモリ１０の１／４セクタをメディアセクタとして割当てている。

【００２９】たとえば、メディアセクタアドレス０ｈは、フラッシュセクタアドレス０ｈのフラッシュカラムアドレス０ｈ～１ＦＦｈに相当する。メディアセクタアドレス１ｈは、フラッシュセクタアドレス０ｈのフラッシュカラムアドレス２００ｈ～３ＦＦｈに相当する。同様に、メディアセクタアドレス２ｈは、フラッシュセクタアドレス０ｈのフラッシュカラムアドレス４００ｈ～５ＦＦｈに相当する。メディアセクタアドレス３ｈは、フラッシュセクタアドレス０ｈのフラッシュカラムアドレス６００ｈ～７ＦＦｈに相当する。つまり、各フラッシュセクタアドレスはそれぞれ４分割され、メディアセクタアドレスに割当てられている。

【００３０】図３は、メディアセクタアドレスをフラッシュセクタアドレスとカラムアドレスオフセット生成ビットとに変換する説明をするための図である。

【００３１】図３を参照して、メディアセクタアドレスＭＡ１５～ＭＡ０の上位１４ビットは、フラッシュセクタアドレスＳＡ１３～ＳＡ０として使用される。また、メディアセクタアドレスのうち下位２ビットであるＭＡ１、ＭＡ０は、カラムアドレスオフセット生成ビットＣ１、Ｃ０として使用され、このカラムアドレスオフセット生成ビットから後に説明するスタートフラッシュカラムアドレスオフセットを発生する。

【００３２】図４は、スタートフラッシュカラムアドレスオフセットとメディアセクタアドレスの下位２ビットとの関係を示す図である。

【００３３】図４を参照して、ＭＡ１、ＭＡ０がともに０であるときは、スタートフラッシュカラムアドレスオフセットは０ｈに設定され、メディアセクタ容量である５１２バイトのデータの授受がバッファメモリとフラッシュメモリとの間で行なわれる。

【００３４】ＭＡ１、ＭＡ０がそれぞれ、０、１であるときは、スタートフラッシュカラムアドレスオフセットは２００ｈに設定され、バッファメモリとフラッシュメモリとの間のデータ授受が行なわれる。

【００３５】ＭＡ１、ＭＡ０がそれぞれ１、０の場合には、スタートフラッシュカラムアドレスオフセットは４００ｈに設定され、バッファメモリとフラッシュメモリとの間でデータ授受が行なわれる。

【００３６】ＭＡ１、ＭＡ０がともに１であるときは、スタートフラッシュカラムアドレスオフセットは６００ｈに設定され、バッファメモリとフラッシュメモリとの間のデータ授受が行なわれる。

【００３７】図５は、実施の形態１の記憶装置の処理のメインフローを示す図である。図５を参照して、ステップＳ０１は、ホストシステムからの要求待ちのステップである。続いて、ステップＳ０２において、読出の要求があったか否かが判断される。読出要求があった場合には、ステップＳ０４に移り、読出処理が行なわれる。読出処理が完了すると、再び、ステップＳ０１に戻りホストシステムからの要求待ち状態となる。

【００３８】ステップＳ０２において、読出要求が行なわれていない場合には、ステップＳ０３に進む。ステップＳ０３では、ホストシステムから書込要求が行なわれていないかどうかが判断される。書込要求があった場合には、ステップＳ０５に進み、書込処理が行なわれる。書込処理が完了すると、再び、ステップＳ０１に進みホストシステムからの要求待ち状態となる。

【００３９】ステップ０３において、書込要求が行なわれなかった場合には、再び、ステップＳ０１に戻り、ホストシステムからの要求待ち状態となる。

【００４０】図６は、図５に示したステップＳ０４の読出処理の詳細を示すフローチャートである。

【００４１】図６を参照して、ステップＳ１１において、読出が開始される。次いで、ステップＳ１２において、メディアセクタアドレスがホストシステムから受信される。続いて、受信したメディアセクタアドレスをもとにアドレス変換が行なわれ、図４で示したスタートフラッシュカラムアドレスオフセットの値が生成される。

【００４２】続いてステップＳ１４において、フラッシュメモリからセクタ読出が行なわれる。そして読出されたデータは、ステップＳ１５において、オフセット値に基づきバッファメモリに書込まれる。続いてステップＳ１６において、ホストシステムに割込み信号を送出し、ステップＳ１７において、バッファメモリに書込まれたデータをホストシステムに対して読出データとして送出する。そしてステップＳ１８において、読出が終了する。

【００４３】図７は、図６に示した読出処理の各ステップが記憶装置内のどのブロックで実施されているかを示す図である。

【００４４】図７を参照して、まずホストシステムからコントローラやバッファメモリに対してメディアセクタアドレスの読出要求が発信される。コントローラというのは、図１におけるホストインタフェイス部２およびフラッシュインタフェイスシーケンサ部６に該当する。

【００４５】これを受けて、コントローラではメディアセクタアドレスからフラッシュメモリのセクタアドレスＳＡとオフセット値の生成がされる。そして、フラッシュメモリに対してリードコマンドとセクタアドレスＳＡが発信される。応じて、フラッシュメモリではセクタリードが行なわれ２０４８バイトのデータが順次フラッシ

ュインタフェイスデータ出力としてコントローラに送出される。これを受けてコントローラではメディアセクタアドレスに基づくオフセットに対応する５１２バイトのデータを抜き出してバッファメモリへと転送する。

【００４６】そしてバッファメモリへのデータの格納が終了すると　コントローラはホストシステムに対してメディアセクタアドレスのデータ読出要求を行ないホストシステムは割込みを受付ける。続いて、コントローラはバッファメモリからデータを出力しこれによりメディアセクタアドレスのデータ読出が行なわれる。そして読出が終了する。

【００４７】図８は、図５に示したステップＳ０５における書込処理の詳細を示すフローチャートである。

【００４８】図８を参照して、まず、ステップＳ２１において書込が開始される。続いて、ステップＳ２２においてホストシステムから発信されたメディアセクタアドレスが受信される。

【００４９】続いて、ステップＳ２３において、記憶装置がホストシステムに対してデータを要求する。そして、ステップＳ２４において、記憶装置がホストシステムからデータを受信する。このデータはステップＳ２５において、バッファメモリに書込まれる。

【００５０】そして、ステップＳ２６において、ステップＳ２２で受信したメディアセクタアドレスからオフセット値の生成がされる。その後、ステップＳ２７においてフラッシュメモリに対するプログラムコマンドの設定がされる。続いて、ステップＳ２８において、バッファメモリからのデータを初期値データと合成し所定のタイミングでフラッシュメモリに書込が行なわれる。

【００５１】そして、ステップＳ２９において書込が終了する。図９は、図８に示した書込処理の各ステップがホストシステムとコントローラおよびバッファメモリとフラッシュメモリとの間でどのように行なわれるかを示す図である。

【００５２】図９を参照して、まずホストシステムからメディアセクタアドレスの書込要求がコントローラに向けて発信される。続いて、コントローラはこれを受けてメディアセクタアドレスへのデータ書込要求をホストシステムに対して行なう。応じてホストシステムはメディアセクタアドレスに対するデータの書込を行なう。このデータはコントローラを経由してバッファメモリに入力される。

【００５３】続いて、コントローラでは受信していたメディアセクタアドレスからフラッシュメモリのセクタアドレスおよびオフセット値の生成がされる。そして、フラッシュメモリに対するプログラムコマンドおよびセクタアドレスの発信がされる。

【００５４】これを受けて、フラッシュメモリはデータ書込可能状態となる。そして、コントローラからの所定の信号に基づきバッファメモリからはオフセット値に基づいて格納されていた５１２バイトのデータが転送される。フラッシュメモリへの書込データが転送されている期間のうち、バッファメモリに格納されていたデータが転送される期間以外の書込データとしては“ＦＦｈ”が転送される。フラッシュメモリへバッファメモリのデータを含む書込データが入力されると、その後、所定のウエイト時間経過後書込が終了する。

【００５５】ここで、書込みデータ“ＦＦｈ”について説明する。フラッシュメモリの各メモリセルは、フローティングゲートを有するＭＯＳトランジスタで構成されている。各メモリセルはＭＯＳトランジスタのしきい値電圧の状態でデータ“１”、“０”を保持している。一般に、メモリセルの消去直後の状態は、保持データ“１”に対応する。データ“０”の書込動作がされるとしきい値電圧が変化し、変化後のしきい値電圧を有するメモリセルの状態が保持データ“０”に対応する。一方、データ“１”の書込動作ではしきい値電圧は変化しない。このため、初期状態としてデータ“０”を保持しているメモリセルに対してデータ“１”の書込動作が行われても、保持データは変化しない。

【００５６】つまり、通常は、メモリセルデータの消去が行なわれてからデータの書込が行なわれるが、実施の形態１では、消去動作を行わずデータとして“ＦＦｈ”を書込む。“ＦＦｈ”はビットがすべて“１”の１バイトのデータであるため、フラッシュメモリは書込む直前のデータを保持するのである。

【００５７】図１０は、図１に示したデータ転送制御部８の詳細を示すブロック図である。図１０を参照して、データ転送制御部８は、記憶装置内部で生成されるリードセクタイネーブル信号ＲＳＥ＃をクロック信号ＳＣの立上がりに同期してラッチするフリップフロップ２２と、フリップフロップ２２の出力と記憶装置内部で生成されるライトセクタイネーブル信号ＷＳＥ＃との論理和をリセット信号ＲＳＴとして出力するＡＮＤ回路２４と、リセット信号ＲＳＴによってリセットされその後クロック信号ＳＣの立上がりに応答してカウントアップを開始するＳＣカウンタ２６と、ホストシステムより１６ビットのメディアセクタアドレスをラッチして上位１４ビットをシーケンサ部６へセクタアドレスＳＡ０～ＳＡ１５として出力するメディアセクタアドレスラッチ部３０と、ＳＣカウンタ２６の出力である１１ビットの計数値のうち上位２ビットとメディアセクタアドレスラッチ部３０がラッチしたメディアセクタアドレスの下位２ビットとを比較する比較器３２とを含む。

【００５８】比較器３２は、ＳＣカウンタ２６からの２ビットのデータとメディアセクタアドレスラッチ部３０からの２ビットのデータとが一致したときにＬレベルとなる比較結果信号をＣＭＰを出力する。

【００５９】データ転送制御部８は、さらに、フリップフロップ２２の出力とクロック信号ＳＣと結果信号ＣＭ

下とを受けてライトイネーブル信号／ＷＥ＃を出力するゲート回路２８と、バッファメモリ４からの出力と固定データ“ＦＦｈ”とを受けて比較結果信号ＣＭＰに応じてフラッシュメモリに対して出力するセレクタ３４とを含む。セレクタ３４は、比較信号ＣＭＰがＬのときはバッファメモリからの出力をフラッシュメモリに対して出力し、比較信号ＣＭＰがＨのときは固定データ“ＦＦｈ”をフラッシュメモリに対して出力する。

【００６０】尚、説明の便宜のため　図１０にはバッファメモリ４が記載されている。バッファメモリ４は、ＳＣカウンタ２６の１１ビットの計数値のうちの下位９ビットをアドレス信号ＡＤＲとして受け、ライトセクタイネーブル信号ＷＳＥ＃をアウトプットイネーブル信号／ＣＥ＃として受け、ゲート回路２８の出力をライトイネーブル信号／ＷＥ＃として受けこれらに応答してフラッシュメモリからのデータ入力ＤＩを受けて保持し、またはセレクタ３４を介してフラッシュメモリへデータ出力ＤＯを送出する。

【００６１】図１１は、フラッシュメモリからバッファメモリへのデータ転送の様子を示すタイミング図である。

【００６２】図１１を参照して、時刻ｔ１からクロック信号ＳＣに応じてデータ信号ＤＡＴＡがフラッシュメモリから読出される。この読出は、セクタ単位で行なわれるため、通常は２０４８データが連続して以後読出される。

【００６３】ここで、ホストシステムから指定されたメディアセクタアドレスのうち最下位の２ビットである（ＭＡ１，ＭＡ０）が（０，１）のときには時刻ｔ１～ｔ２においては、フラッシュメモリから読出されたデータはバッファメモリへは転送されない。

【００６４】そして、時刻ｔ２～ｔ３において、カラムアドレス２００ｈ～３ＦＦｈに相当するデータがフラッシュメモリから読出されている間は、これらのデータはバッファメモリへと転送されて保持される。この保持されるデータは、フラッシュメモリから読出されるセクタ容量２０４８バイトのうちの５１２バイトであり、セクタ容量の４分の１である。

【００６５】時刻ｔ３以降は、カラムアドレス４００ｈ以降のデータが順次読出されるが、これらはバッファメモリへは保持されることはない。

【００６６】図１２は、図１１に示したバッファメモリへのデータ書込の動作をより詳細に示した動作波形図である。

【００６７】図１０、図１２を参照して、時刻ｔ０において、ホストシステムから読出要求が行なわれたことに応じて、リードセクタイネーブル信号ＲＳＥ＃がＨレベルからＬレベルへと立下がる。続いて、時刻ｔ１においてリセット信号ＲＳＴがＨレベルからＬレベルへと立下がり、ＳＣカウンタ２６のリセットが解除される。以

降、時刻ｔ１～ｔ２において、クロック信号ＳＣの入力に応じてＳＣカウンタ２６は１１ビットのカウント値を０ｈから１ＦＦｈまでカウントアップする。カウント値の下位９ビットであるバッファメモリに入力されるアドレス信号ＡＤＲは、同様に０ｈから１ＦＦｈまで変化する。このとき、比較器３２に入力されるカウント値の上位２ビットは（０，０）であり、メディアセクタアドレスラッチ部３０からの２ビットの入力は（０，１）であるため、比較結果信号ＣＭＰは不一致を示すＨレベルである。そのため、データ入力信号ＤＩの内容は、時刻ｔ１～ｔ２においては、バッファメモリ４に書込まれることはない。

【００６８】時刻ｔ２において、ＳＣカウンタ２６のカウント値が２００ｈになり、カウント値の上位２ビットがメディアセクタアドレスラッチ部３０から入力される２ビットの信号と一致する。応じて、比較結果信号ＣＭＰがＨからＬレベルへと立下がる。すなわち、そして、比較結果信号ＣＭＰは、カウント値が２００ｈ～３ＦＦｈである間Ｌレベルとなる。この比較結果信号ＣＭＰの変化に応じて、ゲート回路２８がクロック信号ＳＣをライトイネーブル信号／ＷＥ＃としてバッファメモリに対して出力する。バッファメモリ４は、ライトイネーブル信号／ＷＥ＃が入力されるため、ライトイネーブル信号／ＷＥ＃の立上がりエッジにおけるアドレス信号ＡＤＲが示すアドレスにデータ入力であるデータ０ｈ～データ１ＦＦｈが書込まれる。

【００６９】時刻ｔ３以降においては、ＳＣカウンタ２６のカウント値が４００ｈ以上となるため、比較結果信号ＣＭＰは再びＨレベルになり、以降入力されるデータはバッファメモリへは書込まれない。

【００７０】図１３は、バッファメモリからフラッシュメモリへのデータ転送の様子を示すタイミング図である。

【００７１】図１３を参照して、メディアセクタアドレス（ＭＡ１，ＭＡ０）が（０，１）のときには、時刻ｔ１～ｔ２において、フラッシュメモリのカラムアドレス０ｈ～１ＦＦｈには、ダミーデータである“ＦＦｈ”が書込まれる。このダミーデータは、フラッシュメモリの消去直後の初期値に対応するデータであり、一般に、フラッシュメモリはこの初期値データを書込む動作を行なっても既に内部に保持されているデータが破壊されることはない。

【００７２】したがって、実施の形態１の記憶装置は、一括消去され、その後逐次データを追加していくような用途、例えば、デジタルカメラの画像の一時保存や、携帯型デジタルオーディオ機器の音響信号の保存等に好適に用いられる。

【００７３】時刻ｔ２～ｔ３において、フラッシュメモリのカラムアドレス２００ｈ～３ＦＦｈには、バッファメモリからデータが順次書込まれる。このデータはフラ

ッシュメモリのセクタ容量の１／４に相当する５１２バイトのデータである。

【００７４】時刻ｔ３以降は、時刻ｔ１～ｔ２と同様に、ダミーデータである"ＦＦｈ"が書込まれる。

【００７５】図１４は、図１３に示したバッファメモリからフラッシュメモリへのデータ転送の様子をさらに詳しく説明するための動作波形図である。

【００７６】図１０、図１４を参照して、時刻ｔＣにおいて　ホストシステムからの書込要求に応じてライトセクタイネーブル信号ＷＳＥ＃がＨレベルからＬレベルへと立下がる。応じて、リセット信号ＲＳＴがＨレベルからＬレベルへと立下がり、ＳＣカウンタ２６のリセットが解除される。また、バッファメモリのアウトプットイネーブル入力信号／ＯＥ＝はＨレベルからＬレベルへと立下がり、バッファメモリ４は、アクセス可能な状態となる。

【００７７】時刻ｔ１～ｔ２において、クロック信号ＳＣの立上がりに同期して、セレクタ３４が出力するデータ出力信号がフラッシュメモリへ書込まれる。そのときの書込カラムアドレスに対応するカウント値がＳＣカウンタ２６によってカウントアップされる。時刻ｔ１～ｔ２においてはメディアセクタアドレス（ＭＡ１，ＭＡ０）がＳＣカウンタ２６の上位２ビットと一致しないので、データ出力信号ＤＯはセレクタ３４の"１"側の入力ノードに入力されている固定データ"ＦＦｈ"である。

【００７８】時刻ｔ２において、カウント値の変化に従って、比較結果信号ＣＭＰはＨレベルからＬレベルへと立下がり、アドレス信号ＡＤＲに指定されるアドレスのデータはバッファメモリ４から読出され、セレクタ３４を介してデータ出力信号ＤＯとしてフラッシュメモリへと転送される。以降時刻ｔ３に至るまでの間バッファメモリからフラッシュメモリへとデータ転送が行なわれる。

【００７９】データ０ｈ～データＩＦＦｈの５１２バイトのデータの転送が終了すると、時刻ｔ３において、カウント値の変化に従い比較結果信号ＣＭＰがＬレベルからＨレベルへと立上がるため、再びデータ出力信号はセレクタ３４の"１"側の入力ノードに入力されている固定値"ＦＦｈ"となる。

【００８０】以上説明したように、実施の形態１の記憶装置は、一括消去され、その後逐次データを追加していくような用途、例えば、デジタルカメラの画像の一時保存や、携帯型デジタルオーディオ機器の音響信号の保存等に好適に用いられる。

【００８１】そして、使用するフラッシュメモリの１セクタの容量よりもホストシステムとのデータ転送の単位容量であるメディアセクタ容量が小さい場合に、一時的なデータ格納を行なうバッファメモリの容量をメディアセクタ容量に合わせて小さくすることができるため、ハードウェアを構成する上でコスト的に有利な記憶装置を提供することができる。

【００８２】［実施の形態２］図１５は、実施の形態２の記憶装置５１の概略構成を示すブロック図である。

【００８３】図１５を参照して、記憶装置５１は、ホストシステム１２と記憶する外部データの授受を行なうためのものであり、ホストシステムからメディアアドレスを受けてアドレス変換を行い、ホストシステムの間で外部データを授受するためにデータ変換を行うデータ入出力部５９と、データ入出力部５９が変換したアドレス信号に応じてデータ授受を行うフラッシュメモリ６０とを含む。データ入出力部５９はフラッシュメモリ６０が入出力するデータと外部データとの間のデータの変換を行う。

【００８４】データ入出力部５９は、ホストシステム１２とデータ転送を行なうホストインタフェイス部５２と、ホストインタフェイス部５２がホストシステム１２とデータ転送を行なうために記憶データを一時的に格納する５１２バイトの容量を持つバッファメモリ５４と、ホストインタフェイス部５２からの指令に応じてバッファメモリ５４とフラッシュメモリ６０とのデータ授受のコントロールを行なうフラッシュインタフェイス部５７とを含む。

【００８５】フラッシュインタフェイス部５７は、フラッシュメモリの仕様にあわせたシーケンスで、読出や書込等の動作を設定するコマンドや、読出や書込時にメモリ領域を指定するためのアドレスをフラッシュメモリに送出するシーケンサ部５６と、ホストシステム１２から与えられたメディアセクタアドレスからフラッシュメモリのセクタアドレスとセクタアドレスで指定されたカラムの読出開始位置を指定するスタートカラムアドレスとを生成するカラムアドレス制御部５８とを含む。

【００８６】図１５において、フラッシュメモリ６０は、データのリードおよびプログラムをセクタの任意のカラムアドレスから読出および書込開始をすることができる分割リード／プログラム機能を有する。

【００８７】フラッシュメモリ６０は、各々が２０４８バイトの容量を持つ複数のセクタを有する。フラッシュメモリは、セクタアドレスが指定されると、指定されたセクタ容量分だけのデータをクロック信号に同期してシリアルに出力することができる。そして、スタートカラムアドレスがさらに指定されると、指定されたセクタのカラムアドレスに該当するデータからセクタの最終アドレスに該当するデータまでをクロック信号に同期してシリアルに出力することができる。

【００８８】図１６は、実施の形態２におけるフラッシュメモリとバッファメモリとの対応関係を示すメモリマップである。

【００８９】図１６に示されるメモリマップは、図２に示した実施の形態１に用いられるメモリマップと同様の

割付を示しているため説明は繰返さない。

【００９０】図１７は、メディアセクタアドレスがフラッシュセクタアドレスとスタートカラムアドレスとに変換されることを説明するための図である。

【００９１】図１７を参照して、メディアセクタアドレスＭＡ１５～ＭＡ０の上位１４ビットは、フラッシュセクタアドレスＳＡ１３～ＳＡ０として使用される。また、メディアセクタアドレスのうち下位２ビットであるＭＡ１、ＭＡ０は、スタートカラムアドレスのうちそれぞれＣＡ１０、ＣＡ９として使用される。また、スタートカラムアドレスの他のビットであるＣＡ１１、ＣＡ８～ＣＡ０はすべて"０ｈ"に設定される。

【００９２】図１８は、フラッシュメモリのスタートカラムアドレスとメディアセクタアドレスの下位２ビットとの関係を示す図である。

【００９３】図１８を参照して、ＭＡ１、ＭＡ０がともに０であるときは、スタートカラムアドレスは０ｈに設定され、ＭＡ１、ＭＡ０がそれぞれ０、１であるときは、スタートカラムアドレスは２００ｈに設定される。

【００９４】ＭＡ１、ＭＡ０がそれぞれ１、０であるときは、スタートカラムアドレスは４００ｈに設定され、ＭＡ１、ＭＡ０がともに１であるときは、スタートカラムアドレスは６００ｈに設定される。このアドレス変換は図１５のカラムアドレス制御部５８で行われるが、図１８に対応する配線の接続をするだけで容易に実現できる。

【００９５】図１９は、スタートカラムアドレスの説明をするための概念図である。図１９を参照して、１セクタが２０４８バイトであるときは、フラッシュセクタアドレスＳＡに対応して０ｈ～７ＦＦｈのカラムアドレスが存在する。スタートカラムアドレスＣＡを設定すると、設定したフラッシュセクタアドレスＳＡ中のスタートカラムアドレスに対応するカラムのデータからクロック信号に同期して読出が開始される。

【００９６】図２０は、分割リード／プログラム機能を有するフラッシュメモリからデータを読出す際のコマンド設定とアドレス設定とを説明するための動作波形図である。

【００９７】図２０を参照して、時刻ｔ１において、コマンドデータイネーブル信号／ＣＤＥ＃がＬレベルのときに、ライトイネーブル信号／ＷＥ＃の立上がりが検出されると、そのタイミングにおいて、リードコマンドがフラッシュメモリに取込まれる。

【００９８】時刻ｔ２において、ライトイネーブル信号／ＷＥ＃の立上がりエッジにおいて、セクタアドレスの下位８ビットであるＳＡ（１）が取込まれる。次いで時刻ｔ３において、ライトイネーブル信号／ＷＥ＃の立上がりエッジにおいて、セクタアドレスの上位６ビットであるＳＡ（２）がフラッシュメモリに取込まれる。

【００９９】次いで、時刻ｔ４において、ライトイネーブル信号／ＷＥ＃の立上がりエッジでスタートカラムアドレスＣＡの下位８ビットであるＣＡ（１）がフラッシュメモリに取込まれる。続いて、時刻ｔ５において、ライトイネーブル信号／ＷＥ＃の立上がりエッジでスタートカラムアドレスの上位４ビットであるＣＡ（２）が取込まれる。

【０１００】時刻ｔ６以降は、クロック信号ＳＣに同期してアドレス／データ入出力端子から指定されたスタートカラムアドレスのデータを先頭にしてフラッシュメモリからデータが出力される。

【０１０１】図２１は、実施の形態２においてフラッシュメモリにデータを書込む入力波形を示す図である。

【０１０２】図２１を参照して、時刻ｔ１において、コマンドデータイネーブル入力／ＣＤＥ＃がＬレベルのときに、ライトイネーブル信号／ＷＥ＃の立上がりエッジが検出されると、プログラムコマンドがフラッシュメモリに読込まれる。

【０１０３】続いて、時刻ｔ２において、ライトイネーブル信号／ＷＥ＃の立上がりエッジでセクタアドレスの下位８ビットであるＳＡ（１）がフラッシュメモリに取込まれる。続いて、時刻ｔ３において、ライトイネーブル信号／ＷＥ＃の立上がりエッジでセクタアドレスの上位６ビットであるＳＡ（２）がフラッシュメモリに取込まれる。

【０１０４】時刻ｔ４において、ライトイネーブル信号／ＷＥ＃の立上がりエッジでスタートカラムアドレスの下位８ビットであるＣＡ（１）がフラッシュメモリに取込まれる。続いて、時刻ｔ５において、ライトイネーブル信号／ＷＥ＃の立上がりエッジでスタートカラムアドレスの上位４ビットであるＣＡ（２）がフラッシュメモリに取込まれる。以上でアドレス設定が終了する。

【０１０５】時刻ｔ６以降は、設定されたセクタアドレスのスタートカラムアドレスに対応するデータを先頭としてクロック信号ＳＣに同期してシリアルにデータ入力がされ対応するアドレスにデータが書込まれる。

【０１０６】図２０、図２１で示したフラッシュメモリに対するコマンドやアドレス信号を与える制御は、図１５におけるフラッシュインタフェイスシーケンサ部５６で行なわれる。

【０１０７】図２２は、実施の形態２の記憶装置の処理のメインフローを示す図である。図２２を参照して、実施の形態２の記憶装置の処理のメインフローは、図５に示した実施の形態１の読出処理ステップＳ０４に代えてステップＳ１０４を含み、書込処理ステップＳ０５に代えてステップＳ１０５を含む点が図５で示したフローと異なる。他の部分は図５で示したフローと同様であるので説明は繰返さない。

【０１０８】図２３は、図２２に示したステップＳ１０４の読出処理の詳細を示すフローチャートである。

【０１０９】図２３を参照して、ステップＳ１１１にお

いて、読出が開始される。次いで、ステップＳ１１２において、メディアセクタアドレスがホストシステムから受信される。続いて、ステップＳ１１３において、受信したメディアセクタアドレスを変換してフラッシュメモリのセクタアドレスＳＡおよびスタートカラムアドレスＣＡが発生される。続いて、ステップＳ１１４において、フラッシュメモリの分割リードコマンドが設定されセクタアドレスＳＡおよびスタートカラムアドレスＣＡも指定される。そして、ステップＳ１１５において、データがフラッシュメモリから読出され、バッファメモリに書込まれる。

【０１１０】バッファメモリへの書込が終了すると、ステップＳ１１６においてホストシステムに対して割込信号が送出される。

【０１１１】続いて、ステップＳ１１７において、バッファメモリに書込まれたデータはホストシステムに対して読出データとして送出される。そして、ステップＳ１１８において、読出が終了する。

【０１１２】図２４は、図２３で示した読出処理の各ステップが記憶装置内のどのブロックで実施されているかを示す図である。

【０１１３】図２４を参照して、まずホストシステムからコントローラやバッファメモリに対してメディアセクタアドレスの読出要求が発信される。コントローラというのは、図１５におけるホストインタフェイス部５２およびフラッシュインタフェイスシーケンサ部５６に該当する。

【０１１４】これを受けてコントローラではメディアセクタアドレスからフラッシュメモリのセクタアドレスＳＡとスタートカラムアドレスＣＡとが生成される。そしてコントローラからはリードコマンドとセクタアドレスおよびスタートカラムアドレスとがフラッシュメモリに送出される。応じて、フラッシュメモリでは、分割リード動作が行なわれ、５１２バイトのデータがバッファメモリへと出力される。バッファメモリへのデータ書込が終了すると、コントローラは指定されたメディアセクタアドレスのデータ読出をホストシステムに対して要求する。そして、バッファメモリからはホストシステムに対してデータの読出が行なわれ、読出動作は終了する。

【０１１５】図２５は、図２２に示したステップＳ１０５における書込処理の詳細を示すフローチャートである。

【０１１６】図２５を参照して、まずステップＳ１２１において書込が開始される。続いてステップＳ１２２においてホストシステムから発信されたメディアセクタアドレスが受信される。

【０１１７】続いて、ステップＳ１２３において、記憶装置がホストシステムに対してデータを要求する。そして、ステップＳ１２４においてホストシステムからデータを受信する。このデータは、ステップＳ１２５においてバッファメモリに書込まれる。

【０１１８】そして、ステップＳ１２６において、ステップＳ１２２で受信したメディアセクタアドレスからフラッシュメモリのセクタアドレスＳＡおよびスタートカラムアドレスＣＡが生成される。続いてステップＳ１２７において、フラッシュメモリに対して分割プログラムコマンドが設定され、続いてセクタアドレスＳＡおよびスタートカラムアドレスＣＡの指定がされる。

【０１１９】そして、ステップＳ１２８において、データが、バッファメモリから読出されフラッシュメモリに書込まれる。そしてステップＳ１２９において、データの書込が終了する。

【０１２０】図２６は、図２５に示した書込処理の各ステップがホストシステムとコントローラおよびバッファメモリとフラッシュメモリとの間でどのように行なわれるかを示す図である。

【０１２１】図２６を参照して、まずホストシステムからメディアセクタアドレスの書込要求がコントローラに向けて発信される。続いて、コントローラはこれを受けてメディアセクタアドレスのデータ書込要求をホストシステムに対して行なう。応じてホストシステムはメディアセクタアドレスに対するデータの書込を行なう。このデータはコントローラを経由してバッファメモリに入力される。

【０１２２】続いて、コントローラでは、受信していたメディアセクタアドレスからフラッシュメモリのセクタアドレスＳＡおよびスタートカラムアドレスＣＡが生成される。そして、コントローラがフラッシュメモリに対してプログラムコマンドとセクタアドレス／ＳＡおよびスタートカラムアドレス／ＣＡの設定を行なう。応じて、フラッシュメモリは、分割プログラム動作を行なう。そしてバッファからは５１２バイトのデータがフラッシュメモリに対して入力され、所定のカラムアドレスを先頭にしてデータ書込が行なわれる。フラッシュメモリへバッファメモリから５１２バイトの書込データが入力されると、その後、所定のウエイト時間経過後書込が終了する。

【０１２３】実施の形態２においては、バッファメモリのアドレス制御およびメディアセクタアドレスからフラッシュメモリに与えるアドレス信号の生成は図１５におけるカラムアドレス制御部５８で行なわれる。

【０１２４】図２７は、図１５におけるカラムアドレス制御部５８の詳細を示すブロック図である。

【０１２５】図２７を参照して、カラムアドレス制御部５８は、記憶装置内部で生成されるリードセクタイネーブル信号ＲＳＥ＃をクロック信号ＳＣの立上がりに同期してラッチするフリップフロップ７２と、フリップフロップ７２の出力と記憶装置内部で生成されるライトセクタイネーブル信号ＷＳＥ＃との論理和をリセット信号ＲＳＴとして出力するＡＮＤ回路７４と、リセット信号Ｒ

ＳＴによってリセットされその後クロック信号ＳＣの立上がりに応答してカウントアップを開始する９ビットのＳＣカウンタ７６と、ホストシステムより１６ビットのメディアセクタアドレスをラッチして上位１４ビット、下位２ビットをそれぞれセクタアドレスＳＡ０～ＳＡ１５、スタートカラムアドレスＣＡ０～１としてシーケンサ部６へ出力するメディアセクタアドレスラッチ部３０と、フリップフロップ７２の出力とクロック信号ＳＣとを受けてライトイネーブル信号／ＷＥ＃を出力するゲート回路７８とを含む。

【０１２６】尚、説明の便宜のため　図１０にはバッファメモリ４が記載されている。バッファメモリ４は、ＳＣカウンタ２６の計数値９ビットをアドレス信号ＡＤＲとして受け、ライトセクタイネーブル信号ＷＳＥ＝をアウトプットイネーブル信号／ＯＥ＃として受け、ゲート回路２８の出力をライトイネーブル信号／ＷＥ＝として受けこれらに応答してフラッシュメモリからのデータ入力ＤＩを受けて保持し、またはフラッシュメモリへデータ出力ＤＯを送出する。

【０１２７】以上説明したように、実施の形態２においては、ホストインタフェイス部がホストシステムとデータ転送を行なうときにデータを一時的に格納するバッファメモリの容量をフラッシュメモリの１セクタの容量よりも小さくできるため、コストメリットのある記憶装置を提供することができる。さらに、分割リード／プログラム可能なフラッシュメモリを搭載し使用することで、メディアセクタ単位で読出および再書込が可能である。

【０１２８】今回開示された実施の形態はすべての点で例示であって制限的なものではないと考えられるべきである。本発明の範囲は上記した説明ではなくて特許請求の範囲によって示され、特許請求の範囲と均等の意味および範囲内でのすべての変更が含まれることが意図される。

【０１２９】

【発明の効果】請求項１に記載のフラッシュメモリを搭載する記憶装置は、セクタ読出をするフラッシュメモリを記憶用半導体装置として用いる場合小容量のバッファメモリを搭載するのでコスト的に有利である。

【０１３０】請求項２に記載のフラッシュメモリを搭載する記憶装置は、請求項１に記載のフラッシュメモリを搭載する記憶装置が奏する効果に加えて、ダミーデータとしてフラッシュメモリが消去された直後のデータと同しデータを書込むため、既にデータ保持が行なわれた部分のデータが失われることはない。

【０１３１】請求項３～５に記載のフラッシュメモリを搭載する記憶装置は、請求項１に記載のフラッシュメモリを搭載する記憶装置が奏する効果に加えて、フラッシュメモリのセクタ容量を外部のメディアセクタ容量で区切って使用することができ、効率的にフラッシュメモリを使用することができる。

【０１３２】請求項６～７に記載のフラッシュメモリを搭載する記憶装置は、請求項１に記載のフラッシュメモリを搭載する記憶装置が奏する効果に加えて、セクタデータの読出をする際にも小容量のバッファメモリを使用することができる。

【０１３３】請求項８～１０に記載のフラッシュメモリを搭載する記憶装置は、請求項６に記載のフラッシュメモリを搭載する記憶装置が奏する効果に加えて、フラッシュメモリのセクタ容量を外部のメディアセクタ容量で区切って使用することができ、効率的にフラッシュメモリを使用することができる。

【０１３４】請求項１１～１２に記載のフラッシュメモリを搭載する記憶装置は、小容量のバッファメモリを搭載するのでコスト的に有利であり、さらに、メディアセクタ単位でデータの再書込が可能である。

【図面の簡単な説明】

【図１】　フラッシュメモリを搭載した記憶装置１の概略構成を示すブロック図である。

【図２】　実施の形態１におけるフラッシュメモリとバッファメモリとのアドレスの対応関係を示すメモリマップである。

【図３】　メディアセクタアドレスをフラッシュセクタアドレスとカラムアドレスオフセット生成ビットとに変換する説明をするための図である。

【図４】　スタートフラッシュカラムアドレスオフセットとメディアセクタアドレスの下位２ビットとの関係を示す図である。

【図５】　実施の形態１の記憶装置の処理のメインフローを示す図である。

【図６】　図５に示したステップＳ０４の読出処理の詳細を示すフローチャートである。

【図７】　図６に示した読出処理の各ステップが記憶装置内のどのブロックで実施されているかを示す図である。

【図８】　図５に示したステップＳＣ５における書込処理の詳細を示すフローチャートである。

【図９】　図８に示した書込処理の各ステップがホストシステムとコントローラおよびバッファメモリとフラッシュメモリとの間でどのように行なわれるかを示す図である。

【図１０】　図１に示したデータ転送制御部５の詳細を示すブロック図である。

【図１１】　フラッシュメモリからバッファメモリへのデータ転送の様子を示すタイミング図である。

【図１２】　図１１に示したバッファメモリへのデータ書込の動作をより詳細に示した動作波形図である。

【図１３】　バッファメモリからフラッシュメモリへのデータ転送の様子を示すタイミング図である。

【図１４】　図１３に示したバッファメモリからフラッシュメモリへのデータ転送の様子をさらに詳しく説明す

るための動作波形図である。

【図１５】　実施の形態２の記憶装置５１の概略構成を示すブロック図である。

【図１６】　実施の形態２におけるフラッシュメモリとバッファメモリとの対応関係を示すメモリマップである。

【図１７】　メディアセクタアドレスをフラッシュセクタアドレスとフラッシュカラムアドレスとに変換を説明するための図である。

【図１８】　フラッシュカラムアドレスとメディアセクタアドレスの下位２ビットとの関係を示す図である。

【図１９】　スタートカラムアドレスの説明をするための概念図である。

【図２０】　分割リード／プログラム機能を有するフラッシュメモリからデータを読出す際のコマンド設定とアドレス設定とを説明するための動作波形図である。

【図２１】　実施の形態２においてフラッシュメモリにデータを書込む入力波形を示す図である。

【図２２】　実施の形態２の記憶装置の処理のメインフローを示す図である。

【図２３】　図２２に示したステップＳ１０４の読出処＊

＊理の詳細を示すフローチャートである。

【図２４】　図２３で示した読出処理の各ステップが記憶装置内のどのブロックで実施されているかを示す図である。

【図２５】　図２２に示したステップＳ１０５における書込処理の詳細を示すフローチャートである。

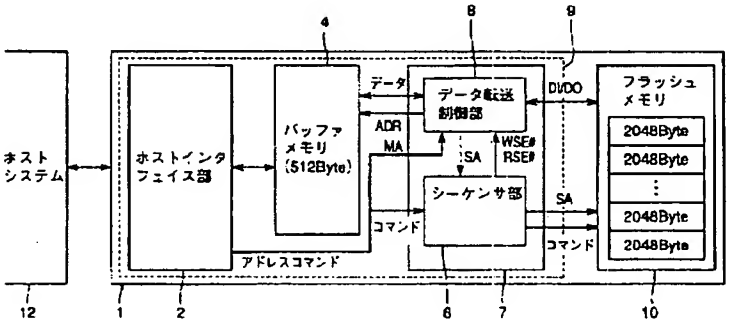
【図２６】　図２５に示した書込処理の各ステップがホストシステムとコントローラおよびバッファメモリとフラッシュメモリとの間でどのように行なわれるかを示す図である。

【図２７】　図１５におけるカラムアドレス制御部５８の詳細を示すブロック図である。

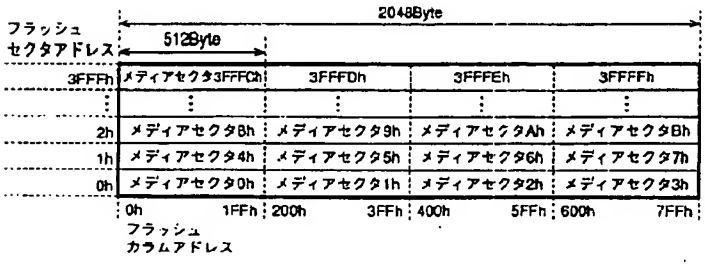
【符号の説明】

１，５１　記憶装置、２，５２　ホストインタフェイス部、４，５４　バッファメモリ、６，５６　フラッシュインタフェイスシーケンサ、８　データ転送制御部、１０，６０　フラッシュメモリ、５８　カラムアドレス制御部、２２　フリップフロップ、２４　ＡＮＤ回路、２６　ＳＣカウンタ、２８　ゲート回路、３０　メディアセクタアドレスラッチ部、３２　比較器、３４　セレクタ。

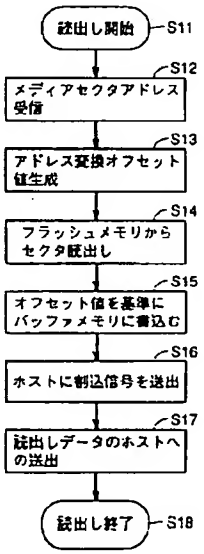
【図１】



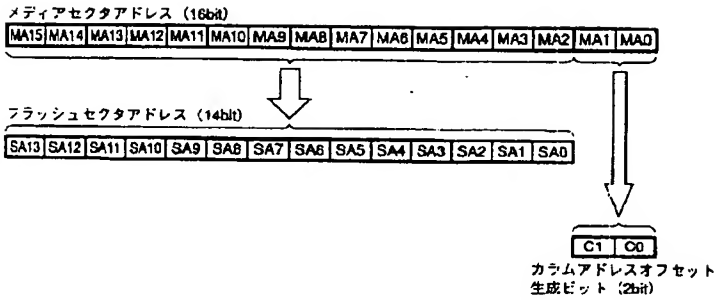
【図２】



【図６】



【図３】

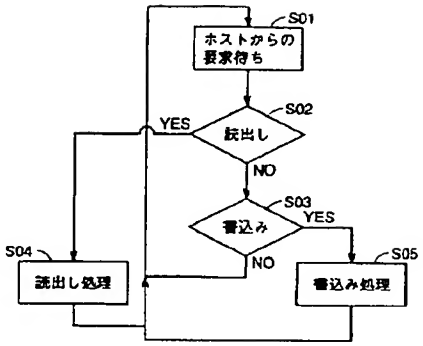


【図４】

◆メディアセクタアドレス（下位2bit）

MA1	MA0	動作
0	0	スタートフラッシュカラムアドレスオフセットを0hとし、512Byteのデータをバッファメモリへ（バッファメモリから）転送する。
0	1	スタートフラッシュカラムアドレスオフセットを200hとし、512Byteのデータをバッファメモリへ（バッファメモリから）転送する。
1	0	スタートフラッシュカラムアドレスオフセットを400hとし、512Byteのデータをバッファメモリへ（バッファメモリから）転送する。
1	1	スタートフラッシュカラムアドレスオフセットを600hとし、512Byteのデータをバッファメモリへ（バッファメモリから）転送する。

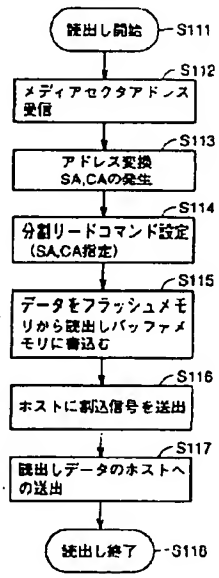
【図５】



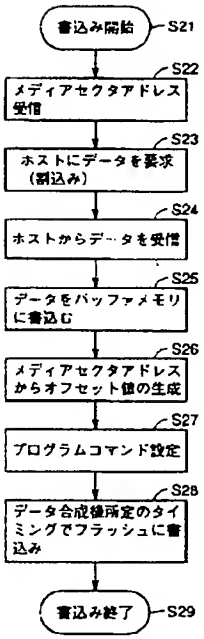
【図７】

HOST	コントローラ（バッファ）	フラッシュメモリ
メディアセクタアドレスxxhの読出し要求	→	
Wait for Interrupt	メディアセクタアドレス → SA,オフセットの生成 ↓ リード・コマンド／SA	→ セクタリード（2048Byte） ↓
	メディアセクタアドレスに基づくオフセットから512Byteのデータをバッファへ転送	← フラッシュ_I/Fデータ出力（2048Byte）
Interrupt ←	メディアセクタアドレスxxhのデータ読出し要求	
メディアセクタアドレスxxhのデータ読出し	← バッファから出力	
読出し終了		

【図２３】



【図８】

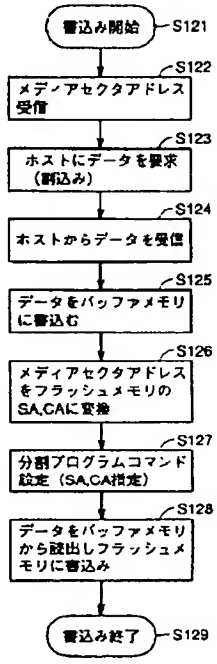


【図９】

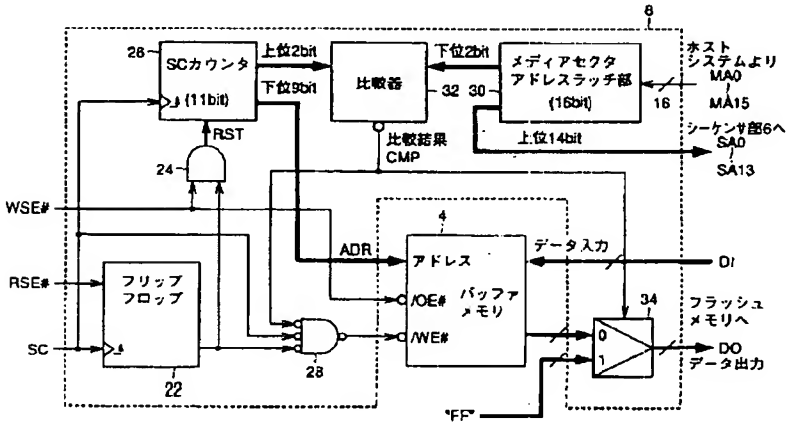
HOST	コントローラ（バッファ）	フラッシュメモリ
メディアセクタアドレス xxhの書込み要求 →		
Interrupt ←	メディアセクタアドレス xxhのデータ書込み要求	
メディアセクタアドレス xxhのデータ書込み →	バッファへ入力	
	メディアセクタアドレス → SA,オフセットの生成 ↓ プログラム・コマンド/SA →	プログラム（2048Byte） ↓
	メディアセクタアドレスに基づくオフセットからバッファのデータを512Byte転送 それ以外ではFFを転送。※ ←	フラッシュへデータ入力（2048Byte） ↓ プログラム__Wait ↓ プログラム__End
書込み終了		

※フラッシュメモリのイレーズ状態がFFである場合。

【図２５】



【図１０】

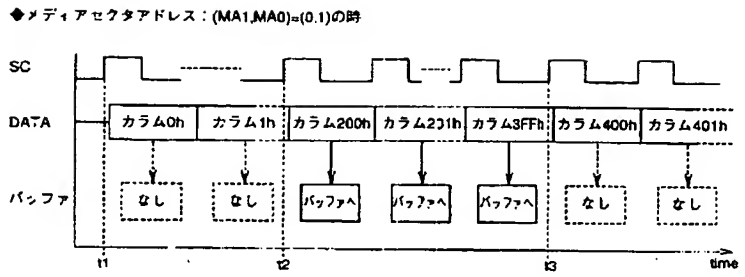


【図１８】

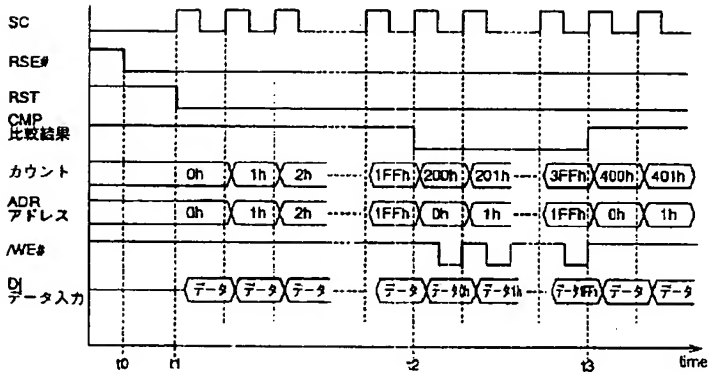
◆メディアセクタアドレス（下位2bit）

MA1	MA0	スタートカラムアドレス
0	0	スタートカラムアドレス：0h
0	1	スタートカラムアドレス：200h
1	0	スタートカラムアドレス：400h
1	1	スタートカラムアドレス：600h

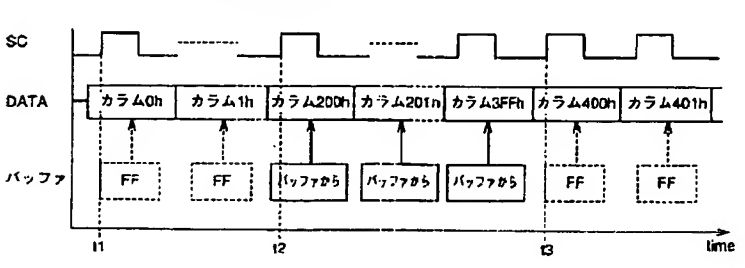
【図１１】


◆メディアセクタアドレス：(MA1,MA0)=(0,1)の時
SC
DATA
カラム0h
カラム1h
カラム200h
カラム201h
カラム3FFh
カラム400h
カラム401h
バッファ
なし
なし
バッファへ
バッファへ
バッファへ
なし
なし
t1
t2
t3
time

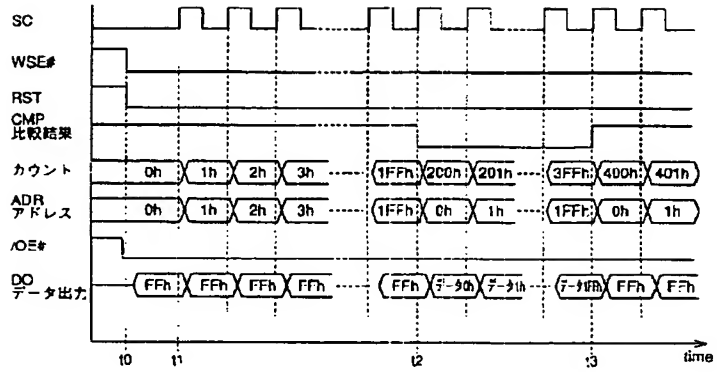
【図１２】


SC
RSE#
RST
CMP
比較結果
カウント
0h
1h
2h
1FFh
200h
201h
3FFh
400h
401h
ADR
アドレス
0h
1h
2h
1FFh
0h
1h
1FFh
0h
1h
/WE#
DI
データ入力
データ
t0
t1
t2
t3
time

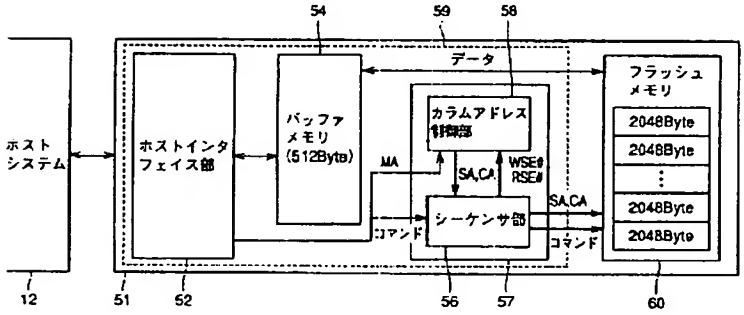
【図１３】


◆メディアセクタアドレス：(MA1,MA0)=(0,1)の時
SC
DATA
カラム0h
カラム1h
カラム200h
カラム201h
カラム3FFh
カラム400h
カラム401h
バッファ
FF
FF
バッファから
バッファから
バッファから
FF
FF
t1
t2
t3
time

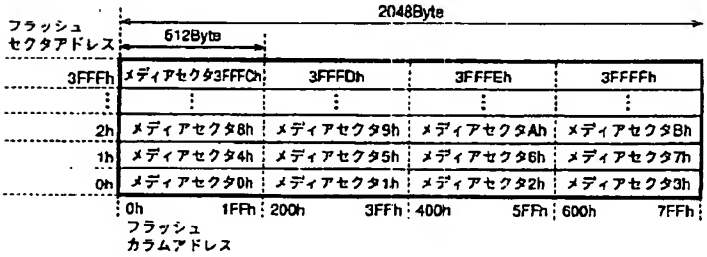
【図１４】


SC
WSE#
RST
CMP
比較結果
カウント
ADR
アドレス
/OE#
DO
データ出力
0h
1h
2h
3h
1FFh
200h
201h
3FFh
400h
401h
FFh
time
t0
t1
t2
t3

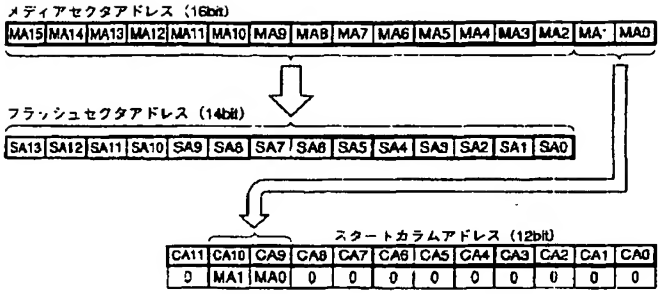
【図１５】


54
59
58
データ
フラッシュ
メモリ
ホスト
システム
ホストインタ
フェイス部
バッファ
メモリ
(512Byte)
MA
カラムアドレス
SA,CA
WSE#
RSE#
シーケンサ部
コマンド
2048Byte
12
51
52
56
57
60

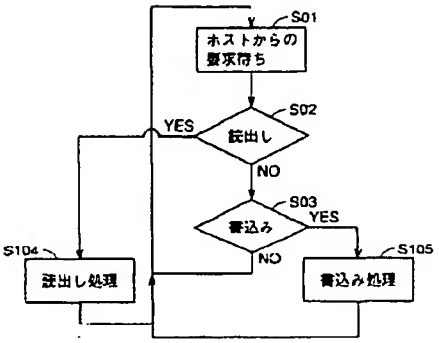
【図１６】


2048Byte
フラッシュ
セクタアドレス
512Byte
3FFFh
メディアセクタ3FFFCh
3FFFDh
3FFFEh
3FFFFh
2h
メディアセクタ8h
メディアセクタ9h
メディアセクタAh
メディアセクタBh
1h
メディアセクタ4h
メディアセクタ5h
メディアセクタ6h
メディアセクタ7h
0h
メディアセクタ0h
メディアセクタ1h
メディアセクタ2h
メディアセクタ3h
0h
1FFh
200h
3FFh
400h
5FFh
600h
7FFh
フラッシュ
カラムアドレス

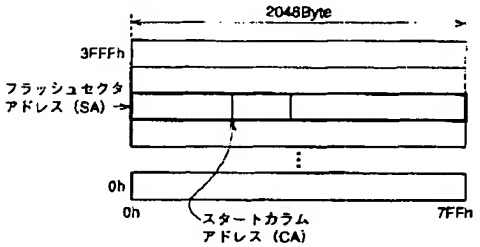
【図１７】



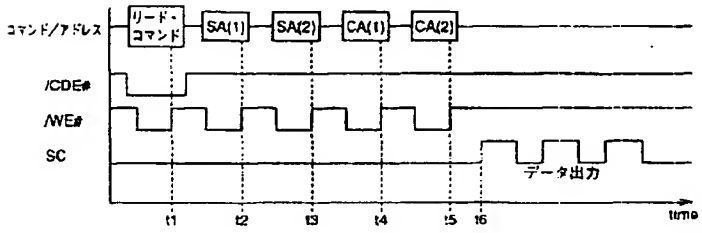
【図２２】



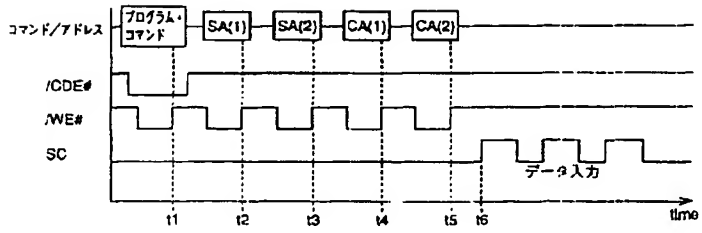
【図１９】



【図２０】



【図２１】



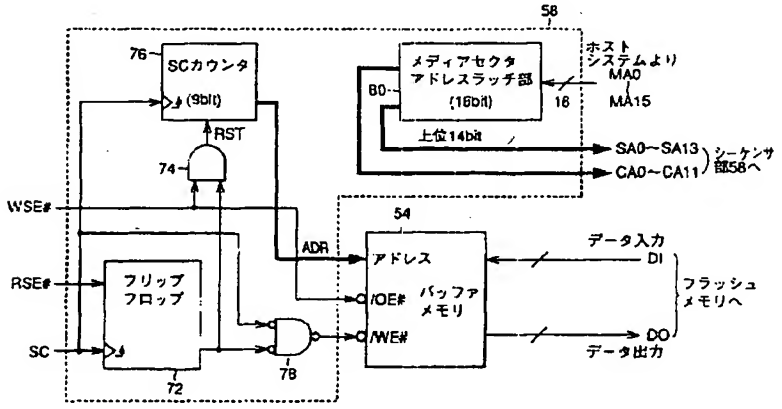
【図24】

HOST	コントローラ（バッファ）	フラッシュメモリ
メディアセクタアドレス xxhの読出し要求 →		
Wait for Interrupt	メディアセクタ → SA,CAの生成アドレス ↓ リード・コマンド/SA/CA →	分割リード（CAによる） ↓ バッファへデータ出力（512Byte）
	512Byteのデータをバッファへ ←	
Interrupt ←	メディアセクタアドレス xxhのデータ読出し要求	
メディアセクタアドレス xxhのデータ読出し ←	バッファから出力	
読出し終了		

【図23】

HOST	コントローラ（バッファ）	フラッシュメモリ
メディアセクタアドレス xxhの書込み要求 →		
Interrupt ←	メディアセクタアドレス xxhのデータ書込み要求	
メディアセクタアドレス xxhのデータ書込み →	バッファへ入力	
	メディアセクタ → SA,CAの生成アドレス ↓ プログラム・コマンド/SA/CA →	分割プログラム（CAによる） ↓ フラッシュへデータ入力（512Byte） ↓ プログラム_Wait ↓ プログラム_End
	512Byteのデータをバッファから ←	
書込み終了		

【図27】



CLAIMS

[Claim(s)]
[Claim 1] It is storage equipped with the write-in mode in which data storage is performed in response to an external write-address signal and an external write data from a host system. Package elimination which makes a smallest unit the memory area holding the data of a predetermined number at the time of data elimination is performed. It has the flash memory by which the store of two or more data is made by making the data length of said predetermined number into a unit. Said flash memory In said write-in mode, incorporate and hold two or more data contained in an internal write data in response to an internal write-address signal, and it sets in said write-in mode. Said internal write-address signal is generated in response to said external write-address signal. Have further the data I/O section which holds in response to said external write data, and outputs said internal write data based on said external write data and said external write-address signal, and said data I/O section is set in said write-in mode. Above the 1st interface section which receives said external write data and said external write-address signal from said host system, and the number of said external write datas And it sets in the buffer memory which has storage capacity smaller than the number of said internal write datas, and receives said external write data from said 1st interface section in said write-in mode, and said write-in mode. In response to said external write-address signal, said internal write-address signal is generated from said 1st interface section. Storage containing the 2nd interface section which adds the dummy data corresponding to said external write-address signal which data rewriting of said memory area does not produce in said external write data read from said buffer memory, and generates said internal write data which carries a flash memory.
[Claim 2] It is the storage which said dummy data is a value corresponding to the data held immediately after carrying out data elimination of said flash memory, and occupies the continuous location where said external write data makes a head location the location corresponding to said external write-address signal in said predetermined sequence by said 2nd interface section outputting serially the data of said data length contained in said internal write data in predetermined sequence and which carries a flash memory according to claim 1.
[Claim 3] Said head location is storage which is discontinuously determined on the basis of [of said predetermined sequence] the 1st by making into a unit the number of data contained in said external write data according to said external write-address signal and which carries a flash memory according to claim 2.
[Claim 4] The number of data contained in said internal write data is storage which is the integral multiple of the number of data contained in said external write data and which carries a flash memory according to claim 3.
[Claim 5] Said flash memory incorporates said internal write data one by one synchronizing with a clock. Said 2nd interface section Generate the read-out control signal over said buffer memory, and said internal write data is generated in response to said external write data from said buffer memory. It has the data transfer control section which generates said internal write-address signal from said external write-address signal. Said data transfer control section When the store of said internal write data is started by said flash memory The comparator which outputs a coincidence signal when a predetermined number bit is in agreement from the high order of the counted value of the counter which starts the count of said clock, and the offset signal included in said external write-address signal and said counter, The gate circuit which gives a read-out control signal to said buffer memory according to said coincidence signal so that said buffer memory may output said external write data synchronizing with said clock, When said coincidence signal is deactivated, the value corresponding to the initial value after elimination of said flash memory is given to said flash memory. It is the storage which has the selection circuitry which gives said external write data read from said buffer memory when said coincidence signal was activated to said flash memory and which carries a flash memory according to claim 2.
[Claim 6] Said storage is further equipped with the read-out mode which outputs external read-out data to said host system in response to an external read-out address signal from said host system. Said data I/O section At the time of the aforementioned read-out mode, in response to said external read-out address signal, generate an internal read-out address signal, and it gives said flash memory. After choosing some internal read-out data read from said flash memory and holding as said external read-out data, Said external read-out data are outputted to said host system. Said 1st interface section At the time of the aforementioned read-out mode, said external read-out data according to the carrier beam aforementioned external read-out address signal are outputted to said host system from said host system. Said buffer memory Are more than the number of said external read-out data, and it has storage capacity smaller than the number of said internal read-out data. Said external read-out data currently held to said 1st interface section at the time of the aforementioned read-out mode are outputted. Said 2nd interface section Two or more data which generate said internal read-out address signal in response to said external read-out

address signal from said 1st interface section, give to said flash memory, and said internal read-out data contain from said flash memory at the time of the aforementioned read-out mode Read-out, Storage which is sent out to buffer memory by using said some of internal read-out data as said external read-out data and which carries a flash memory according to claim 1.

[Claim 7] For said flash memory, said external read-out data are storage which carries the flash memory according to claim 6 which occupies the continuous location which makes [in / output serially the data of said data length contained in said internal read-out data according to said internal read-out address signal in predetermined sequence, and / said predetermined sequence] a head location the location corresponding to said external read-out address signal.

[Claim 8] Said head location is storage which is discontinuously determined on the basis of [of said predetermined sequence] the 1st by making into a unit the number of data contained in said external read-out data according to said external read-out address signal and which carries a flash memory according to claim 7.

[Claim 9] The number of data contained in said internal write data is storage which is the integral multiple of the number of data contained in said external write data and which carries a flash memory according to claim 8.

[Claim 10] Said flash memory carries out the sequential output of said internal read-out data synchronizing with a clock. Said 2nd interface section Said internal read-out address signal is generated from said external read-out address signal. Generate a write control signal to buffer memory so that said some of internal read-out data may be chosen and said buffer memory may store as said external read-out data. It has a data transfer control section. Said data transfer control section When read-out of said internal read-out data is started from said flash memory The comparator which outputs a coincidence signal when a predetermined number bit is in agreement from the high order of the counted value of the counter which starts the count of said clock, and the offset signal included in said external write-address signal and said counter, Have the gate circuit which gives said write control signal to said buffer memory according to said coincidence signal so that said buffer memory may store said some of internal read-out data as said external read-out data synchronizing with said clock. Storage which carries a flash memory according to claim 7.

[Claim 11] The data I/O section which generates the internal main address corresponding to [are the storage which performs data storage which delivers and receives external data in response to an external address signal from a host system, and] said external address, and the internal secondary address, Package elimination which makes a smallest unit the memory area holding the data of a predetermined number at the time of data elimination is performed. Selection of said memory area unit is performed by said internal main address, and it has the flash memory which can deliver and receive serially the in-house data which the data transfer starting position in said memory area is specified, and contains two or more data with said internal secondary address. The storage capacity of said memory area It is the storage which is discontinuously generated on the basis of the start address of said memory area by making into a unit the number of data which is larger than the number of data contained in said external data, and by which said internal secondary address is included in said external write data and which carries a flash memory.

[Claim 12] Said data I/O section is storage containing the buffer memory which has the memory capacity corresponding to the number of data contained in said external data which hold temporarily said external data and said in-house data in order to carry out timing adjustment between said host systems and said flash memories which carries a flash memory according to claim 11.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] More specifically, this invention relates to the storage which carries a flash memory about storage.
[0002]
[Description of the Prior Art] In recent years, the storage capacity of a flash memory is also becoming large with the advance of a semi-conductor manufacturing technology. With this large-capacity-izing, it is small and the storage which carried the flash memory as an archive medium in the field of a pocket device especially taking advantage of the property which is a low power has come to be used.
[0003]
[Problem(s) to be Solved by the Invention] A flash memory is nonvolatile and is the semiconductor memory which can perform rewrting after package elimination. In order to accumulate a storage element on high density and to carry out data transfer to a high speed, a sector address is specified, per sector, the data of a constant rate are put in block and, as for a flash memory, read-out, elimination, and a store (program) are performed for them. Being [for example,] in the inclination which the sector capacity which is the unit as for which a flash memory reads data collectively also increases with large-capacity-izing of a flash memory, by the 256M bit AND mold flash memory, this sector capacity has become 2048 bytes.
[0004] the data volume (in this description, media sector capacity is called henceforth) of the unit at the time of on the other hand the information machines and equipment which make a personal computer the start performing data transfer with stores, such as a hard disk and a memory card, -- for example, it is 512 bytes standardly and the inclination which especially this media sector capacity increases is not seen.
[0005] It is necessary to store the sector data of a flash memory temporarily and to carry the buffer memory for performing timing for performing data transfer with a host system, and adjustment of capacity in the interior of a store in the store which carries such a flash memory with a sector structure. As for this buffer memory, SRAM (Static Random Access Memory) etc. is usually used.
[0006] Rather than the sector capacity of a flash memory, even when it was small capacity, the capacity, i.e., the media sector capacity, of data transfer with a host system, it needed to make capacity of buffer memory the sector capacity of a flash memory, this capacity, or the capacity beyond it.
[0007] However, the sector capacity of a flash memory had large-capacity-ized every year, in such a case, mass SRAM needed to be carried as buffer memory, and the demerit had arisen in cost in it.
[0008] It is offering the storage which carries the flash memory which this invention's was made as [solve / such a trouble], and the object's made it possible to carry the buffer memory of the small capacity equivalent to media sector capacity, and aimed at the cost cut.
[0009]
[Means for Solving the Problem] The storage which carries a flash memory according to claim 1 It is storage equipped with the write-in mode in which data storage is performed in response to an external write-address signal and an external write data from a host system. Package elimination which makes a smallest unit the memory area holding the data of a predetermined number at the time of data elimination is performed. It has the flash memory by which the store of two or more data is made by making the data length of a predetermined number into a unit. A flash memory In write-in mode, incorporate and hold two or more data contained in an internal write data in response to an internal write-address signal, and it sets in write-in mode. It has further the data I/O section which generates an internal write-address signal in response to an external write-address signal, holds in response to an external write data, and outputs an internal write data based on an external write data and an external write-address signal. The data I/O sections are the 1st interface section which receives an external write data and an external write-address signal from a host system in write-in mode, and more than the number of external write datas. And it sets in the buffer memory which has memory capacity smaller than the number of internal write datas, and receives an external write data from the 1st interface section in write-in mode, and write-in mode. In response to an external write-address signal, an internal write-address signal is generated from the 1st interface section. The 2nd interface section which adds the dummy data corresponding to the external write-address signal which data rewriting of a memory area does not produce in the external write data read from buffer memory, and generates an internal write data is included.
[0010] The storage which carries a flash memory according to claim 2 In the configuration of the store which carries a flash

memory according to claim 1 dummy data It is a value corresponding to the data held immediately after carrying out data elimination of the flash memory. The 2nd interface section Outputting serially the data of the data length contained in an internal write data in predetermined sequence, an external write data occupies the continuous location which makes a head location the location corresponding to an external write-address signal in predetermined sequence.

[0011] The storage which carries a flash memory according to claim 3 makes a unit the number of data by which a head location is included in an external write data in the configuration of the storage which carries a flash memory according to claim 2 according to an external write-address signal, and it is discontinuously determined on the basis of [of predetermined sequence] the 1st.

[0012] The number of data by which the storage which carries a flash memory according to claim 4 is contained in an internal write data in the configuration of the storage which carries a flash memory according to claim 3 is the integral multiple of the number of data contained in an external write data.

[0013] The storage which carries a flash memory according to claim 5 In the configuration of the storage which carries a flash memory according to claim 2, in addition, a flash memory Synchronizing with a clock, an internal write data is incorporated one by one. The 2nd interface section Generate the read-out control signal over buffer memory, and an internal write data is generated in response to an external write data from buffer memory. It has the data transfer control section which generates an internal write-address signal from an external write-address signal. A data transfer control section The counter which starts the count of a clock when the store of an internal write data is started by the flash memory, The comparator which outputs a coincidence signal when a predetermined number bit is in agreement from the high order of the counted value of the offset signal included in an external write-address signal, and a counter, The gate circuit which gives a read-out control signal to buffer memory according to a coincidence signal so that buffer memory may output an external write data synchronizing with a clock, When the coincidence signal is deactivated, the value corresponding to the initial value after elimination of a flash memory is given to a flash memory, and when a coincidence signal is activated, it has the selection circuitry which gives the external write data read from buffer memory to a flash memory.

[0014] The storage which carries a flash memory according to claim 6 It adds to the configuration of the storage which carries a flash memory according to claim 1. It has further the read-out mode which outputs external read-out data to a host system in response to an external read-out address signal from a host system. The data I/O section At the time of read-out mode, in response to an external read-out address signal, generate an internal read-out address signal, and it gives a flash memory. After choosing some internal read-out data read from a flash memory and holding as external read-out data, External read-out data are outputted to a host system. The 1st interface section At the time of read-out mode, the external read-out data according to a carrier beam external read-out address signal are outputted to a host system from a host system. Buffer memory Are more than the number of external read-out data, and it has storage capacity smaller than the number of internal read-out data. The external read-out data currently held to the 1st interface section at the time of read-out mode are outputted. The 2nd interface section Two or more data which generate an internal read-out address signal in response to an external read-out address signal from the 1st interface section, give to a flash memory, and internal read-out data contain from a flash memory at the time of read-out mode Read-out, It sends out to buffer memory by using some internal read-out data as external read-out data.

[0015] In addition to the configuration of the storage with which the storage which carries a flash memory according to claim 7 carries a flash memory according to claim 6, a flash memory outputs serially the data of the data length contained in internal read-out data according to an internal read-out address signal in predetermined sequence, and external read-out data occupy the continuous location which makes a head location the location corresponding to an external read-out address signal in predetermined sequence.

[0016] In the configuration of the storage with which the storage which carries a flash memory according to claim 8 carries a flash memory according to claim 7, a head location is discontinuously determined on the basis of [of predetermined sequence] the 1st by making into a unit the number of data contained in external read-out data according to an external read-out address signal.

[0017] The number of data by which the storage which carries a flash memory according to claim 9 is contained in an internal write data in the configuration of the storage which carries a flash memory according to claim 8 is the integral multiple of the number of data contained in an external write data.

[0018] The storage which carries a flash memory according to claim 10 In the configuration of the storage which carries a flash memory according to claim 7, in addition, a flash memory Synchronizing with a clock, the sequential output of the internal read-out data is carried out. The 2nd interface section Generate an internal read-out address signal from an external read-out address signal, and generate a write control signal to buffer memory so that some internal read-out data may be chosen and buffer memory may store as external read-out data. It has a data transfer control section. A data transfer control section The counter which starts the count of a clock when read-out of internal read-out data is started from a flash memory, The comparator which outputs a coincidence signal when a predetermined number bit is in agreement from the high order of the counted value of the offset signal included in an external write-address signal, and a counter, It has the gate circuit which gives a write control signal to buffer memory according to a coincidence signal so that buffer memory may store some internal read-out data as external read-out data synchronizing with a clock.

[0019] The storage which carries a flash memory according to claim 11 The data I/O section which generates the internal main address corresponding to [are the storage which performs data storage which delivers and receives external data in response to an external address signal from a host system, and] the external address, and the internal secondary address,

Package elimination which makes a smallest unit the memory area holding the data of a predetermined number at the time of data elimination is performed. Selection of a memory area unit is performed by the internal main address, and it has the flash memory which can deliver and receive serially the in-house data which the data transfer starting position in a memory area is specified, and contains two or more data with the internal secondary address. The memory capacity of a memory area is larger than the number of data contained in external data, and the internal secondary address is discontinuously generated on the basis of the start address of a memory area by making into a unit the number of data contained in an external write data.
[0020] In addition to the configuration of the storage with which the storage which carries a flash memory according to claim 12 carries a flash memory according to claim 11, the data I/O section contains the buffer memory which has the memory capacity corresponding to the number of data contained in the external data which hold external data and an in-house data temporarily, in order to carry out timing adjustment between a host system and a flash memory.
[0021]
[Embodiment of the Invention] The gestalt of operation of this invention is explained in detail, referring to a drawing below. In addition, a same-among drawing sign shows the same or a considerable part.
[0022] [Gestalt 1 of operation] drawing 1 is the block diagram showing the outline configuration of the store 1 which carried the flash memory.
[0023] With reference to drawing 1 , it is for delivering and receiving the external data remembered to be a host system 12, a store 1 performs address translation in response to the media address from a host system, and in order to deliver and receive external data between host systems, it contains the data I/O section 9 which performs data conversion, and the flash memory 10 which performs data transfer according to the address signal which the data I/O section 9 changed. The data I/O section 9 changes the data between the data and external data which a flash memory 10 outputs and inputs.
[0024] The data I/O section 9 contains a host system, the host interface section 2 which performs data transfer, the buffer memory 4 which has the capacity of 512 bytes which stores some sector data of a flash memory temporarily in order that the host interface section 2 may perform a host system 12 and data transfer, the flash plate interface section 7 which controls data transfer with buffer memory 4 and a flash memory according to the command from the host interface section 2, and the flash memory 10 which is a semiconductor device holding the data which a store 1 should memorize.
[0025] The flash plate interface section 7 is the sequence united with the specification of a flash memory, and contains the data transfer control section 8 which generates the sector address of a flash memory, and column address offset from the sequencer section 6 which sends out the address for specifying a memory area at the time of the command, read-out, and the store which set up actuation of read-out, a store, etc. to a flash memory, and the media sector address given from the host system 12.
[0026] A flash memory 10 has two or more sectors with the capacity whose each is 2048 bytes. A flash memory 10 can output serially 2048 bytes of data memorized by the specified sector, if a sector address is specified.
[0027] Drawing 2 is a memory map in which the response relation of the address of the flash memory and buffer memory in the gestalt 1 of operation is shown.
[0028] With reference to drawing 2 , 512 bytes and 1 sector of a flash memory 10 are the memory rises in the case of being 2048 bytes, and media sector capacity, i.e., the sector capacity which performs [a store 1] data transfer collectively, is assigning 1/4 sector of a flash memory 10 as a media sector.
[0029] For example, it is equivalent to flash plate sector-address 0h flash plate column address 0h-1FFh media sector-address 0h. Media sector-address 1h, it is equivalent to flash plate sector-address 0h flash plate column address 200h-3FFh. Similarly, it is equivalent to flash plate sector-address 0h flash plate column address 400h-5FFh media sector-address 2h. Media sector-address 3h, it is equivalent to flash plate sector-address 0h flash plate column address 600h-7FFh. That is, each flash plate sector address is quadrisected, respectively, and is assigned to the media sector address.
[0030] Drawing 3 is drawing for giving explanation which changes a media sector address into a flash plate sector address and a column address offset generation bit.
[0031] With reference to drawing 3 , 14 bits of high orders of the media sector addresses MA15-MA0 are used as flash plate sector addresses SA13-SA0. Moreover, MA1 and MA0 which are 2 bits of low order among media sector addresses are used as column address offset generation bits C1 and C0, and it generates the start flash plate column address offset later explained from this column address offset generation bit.
[0032] Drawing 4 is drawing showing 2 bits [of low order of start flash plate column address offset and a media sector address] relation.
[0033] With reference to drawing 4 , when both MA1 and MA0 are 0, start flash plate column address offset is set as 0h, and transfer of 512 bytes of data which are media sector capacity is performed between buffer memory and a flash memory.
[0034] When MA1 and MA0 are 0 and 1, respectively, start flash plate column address offset is set as 200h, and data transfer between buffer memory and a flash memory is performed.
[0035] When MA1 and MA0 are 1 and 0, respectively, start flash plate column address offset is set as 400h, and data transfer is performed between buffer memory and a flash memory.
[0036] When both MA1 and MA0 are 1, start flash plate column address offset is set as 600h, and data transfer between buffer memory and a flash memory is performed.
[0037] Drawing 5 is drawing showing the Maine flow of processing of the storage of the gestalt 1 of operation. With reference to drawing 5 , step S01 is a step of the waiting for the demand from a host system. Then, it is judged in step S02 whether there was any demand of read-out. When there is a read-out demand, it moves to step S04 and read-out processing is

performed. If read-out processing is completed, it will be in the state waiting for a demand from a return host system to step S01 again.

[0038] In step S02, when the read-out demand is not performed, it progresses to step S03. At step S03, it is judged whether the write-in demand is performed from the host system. When there is a write-in demand, it progresses to step S05 and write-in processing is performed. If write-in processing is completed, again, it progresses to step S01 and will be in the state waiting for a demand from a host system.

[0039] In step 03, when a write-in demand is not performed, it will be in return and the state waiting for a demand from a host system to step S01 again.

[0040] Drawing 6 is a flow chart which shows the detail of read-out processing of step S04 shown in drawing 5 .

[0041] With reference to drawing 6 , read-out is started in step S11. Subsequently, in step S12, a media sector address is received from a host system. Then, address translation is performed based on the media sector address which received, and the value of the start flash plate column address offset shown by drawing 4 is generated.

[0042] Then, in step S14, sector read-out is performed from a flash memory. And the read data are written in buffer memory in step S15 based on an offset value. Then, in step S16, an interrupt signal is sent out to a host system and the data written in buffer memory are sent out as read-out data to a host system in step S17. And read-out is completed in step S18.

[0043] Drawing 7 is drawing showing with which block in a store each step of the read-out processing shown in drawing 6 is carried out.

[0044] With reference to drawing 7 , the read-out demand of a media sector address is first sent from a host system to a controller or buffer memory. A controller corresponds to the host interface section 2 and the flash plate interface sequencer section 6 in drawing 1 .

[0045] In response by the controller, generation of an offset value is considered as the sector address SA of a flash memory from a media sector address. And a lead command and a sector address SA are sent to a flash memory. It responds, and in a flash memory, a sector lead is performed and the data which are 2048 bytes are sent out to a controller as flash plate interface data output one by one. In response, by the controller, 512 bytes of data corresponding to the offset based on a media sector address are extracted, and it transmits to buffer memory.

[0046] And after storing of the data to buffer memory is completed, a controller performs the data read-out demand of a media sector address to a host system, and a host system receives interruption. Then, a controller outputs data from buffer memory and, thereby, data read-out of a media sector address is performed. And read-out is completed.

[0047] Drawing 8 is a flow chart which shows the detail of the write-in processing in step S05 shown in drawing 5 .

[0048] With reference to drawing 8 , a store is first started in step S21. Then, the media sector address sent from the host system in step S22 is received.

[0049] Then, in step S23, a store requires data from a host system. And in step S24, a store receives data from a host system. This data is written in buffer memory in step S25.

[0050] And in step S26, generation of an offset value is carried out from the media sector address which received at step S22. Then, in step S27, setting out of the program command to a flash memory is carried out. Then, in step S28, the data from buffer memory are compounded with initial value data, and a store is performed to a flash memory to predetermined timing.

[0051] And a store is completed in step S29. Drawing 9 is drawing showing how each step of the write-in processing shown in drawing 8 is performed between a host system, a controller and buffer memory, and a flash memory.

[0052] With reference to drawing 9 , the write-in demand of a media sector address is first sent towards a controller from a host system. Then, in response, a controller gives the data write-in demand to a media sector address to a host system. Responding, a host system writes in the data to a media sector address. This data is inputted into buffer memory via a controller.

[0053] Then, by the controller, generation of the sector address of a flash memory and an offset value is carried out from the media sector address which had received. And dispatch of the program command and sector address to a flash memory is carried out.

[0054] In response, a flash memory will be in the condition which can be data written in. And based on the predetermined signal of a controller, 512 bytes of data stored based on the offset value are transmitted from buffer memory. "FFh" is transmitted as write datas other than the period when the data stored in buffer memory among the periods when the write data to a flash memory is transmitted are transmitted. If the write data containing the data of buffer memory is inputted into a flash memory, the predetermined store after weight time amount progress will be completed after that.

[0055] Here, write-in data "FFh" are explained. Each memory cell of a flash memory consists of MOS transistors which have the floating gate. Each memory cell holds data "1" and "0" in the state of the threshold electrical potential difference of an MOS transistor. Generally, the condition immediately after elimination of a memory cell corresponds to maintenance data "1." If write-in actuation of data "0" is carried out, a threshold electrical potential difference will change, and the condition of a memory cell of having a threshold electrical potential difference after change corresponds to maintenance data "0." On the other hand, a threshold electrical potential difference does not change in write-in actuation of data "1." For this reason, even if write-in actuation of data "1" is performed to the memory cell which holds data "0" as an initial state, maintenance data do not change.

[0056] That is, although the store of data is usually performed after elimination of memory cell data is performed, with the gestalt 1 of operation, elimination actuation is not performed but "FFh" is written in as data. Since "FFh" is data all whose bits are 1 byte of "1", a flash memory holds data just before writing in.

[0057] Drawing 10 is the block diagram showing the detail of the data transfer control section 8 shown in drawing 1 . The flip-flop 22 which latches lead sector enable signal RSE** by which the data transfer control section 8 is generated inside a store with reference to drawing 10 synchronizing with the start of clock signal SC, AND circuit 24 which outputs the OR of the output of a flip-flop 22, and light-sector enable signal WSE** generated inside a store as a reset signal RST, The SC counter 26 which is reset by the reset signal RST, answers the start of clock signal SC after that, and starts count-up, The media sector-address latch section 30 which latches a 16-bit media sector address and outputs 14 bits of high orders to the sequencer section 6 as sector addresses SA0-SA15 from a host system, The comparator 32 which compares 2 bits of high orders with 2 bits of low order of the media sector address which the media sector-address latch section 30 latched among the enumerated data of 11 bits which are the outputs of the SC counter 26 is included.
[0058] A comparator 32 outputs CMP for the comparison result signal used as L level, when the 2 bits data from the SC counter 26 and the 2-bit data from the media sector-address latch section 30 are in agreement.
[0059] The data transfer control section 8 contains further the output of a flip-flop 22, clock signal SC, the gate circuit 28 that outputs a write enable signal / WE** in response to Signal CMP a result, and the output from buffer memory 4 and the selector 34 outputted to a flash memory according to the comparison result signal CMP in response to fixed data "FFh." A selector 34 outputs the output from buffer memory to a flash memory, when the comparison signal CMP is H, it outputs fixed data "FFh" to a flash memory.
[0060] In addition, buffer memory 4 is indicated by drawing 10 for the facilities of explanation. Buffer memory 4 receives 9 bits of low order of the enumerated data of 11 bits of the SC counter 26 as address signal ADR, receives light-sector enable signal WSE** as an output enable signal /OE**, undergoes the output of a gate circuit 28 as a write enable signal /WE**, answers these, and is held in response to data input DI from a flash memory, or sends out data output DO to a flash memory through a selector 34.
[0061] Drawing 11 is the timing chart showing the situation of the data transfer from a flash memory to buffer memory.
[0062] With reference to drawing 11 , data signal DATA is read from a flash memory according to time of day t1 to clock signal SC. Since it is carried out per sector, this read-out is read after 2048 data usually continue.
[0063] the least significant 2 bits among the media sector addresses specified from the host system here -- it is (MA1, MA0) -- when it is (0, 1), in time of day t1-t2, the data read from the flash memory are not transmitted to buffer memory.
[0064] And in time of day t2-t3, while the data equivalent to column address 200h-3FFh are read from the flash memory, these data are transmitted to buffer memory and held. This data held is 512 bytes of 2048-byte sector capacity read from a flash memory, and is the quadrant of sector capacity.
[0065] Although the data after column address 400h are read after time of day t3 one by one, these are not held to buffer memory.
[0066] Drawing 12 is the wave form chart of operation having shown more actuation of the data store to the buffer memory shown in drawing 11 in the detail.
[0067] With reference to drawing 10 and drawing 12 , lead sector enable signal RSE** falls from H level to L level in time of day t0 according to the read-out demand having been performed from the host system. Then, in time of day t1, reset of a fall and the SC counter 26 is canceled for a reset signal RST of H level to L level. Henceforth, in time of day t1-t2, the SC counter 26 counts up the counted value of 11 bits from 0h to 1FFh according to the input of clock signal SC. Address signal ADR inputted into the buffer memory which is 9 bits of low order of counted value changes from 0h to 1FFh similarly. Since 2 bits of high orders of the counted value inputted into a comparator 32 at this time are (0, 0) and the 2-bit inputs from the media sector-address latch section 30 are (0, 1), the comparison result signal CMP is H level which shows an inequality. Therefore, the content of data in signal DI is not written in buffer memory 4 in time of day t1-t2.
[0068] In time of day t2, the counted value of the SC counter 26 is set to 200h, and 2 bits of high orders of counted value are in agreement with the 2-bit signal inputted from the media sector-address latch section 30. It responds and the comparison result signal CMP falls from H to L level. namely, -- and the comparison result signal CMP serves as L level, while counted value is 200h-3FFh. According to change of this comparison result signal CMP, a gate circuit 28 makes clock signal SC a write enable signal /WE**, and outputs to buffer memory. Data 0h- data 1FFh which is a data input is written in the address with which address signal ADR in the start edge of a write enable signal / WE** shows buffer memory 4 since a write enable signal / WE** is inputted.
[0069] Since the counted value of the SC counter 26 is set to 400h or more after time of day t3, the comparison result signal CMP is again set to H level, and the data inputted henceforth are not written in buffer memory.
[0070] Drawing 13 is the timing chart showing the situation of the data transfer from buffer memory to a flash memory.
[0071] With reference to drawing 13 , when media sector addresses (MA1, MA0) are (0, 1), in time of day t1-t2, "FFh" which is dummy data is written in column address 0h-1FFh of a flash memory. This dummy data is data corresponding to the initial value immediately after elimination of a flash memory, and generally, even if a flash memory performs actuation which writes in this initial value data, the data already held inside are not destroyed.
[0072] Therefore, the store of the gestalt 1 of operation is used suitable for momentary preservation of an application which package elimination is carried out and adds data serially after that, for example, the image of a digital camera, preservation of the acoustic signal of a pocket mold digital audio device, etc.
[0073] In time of day t2-t3, data are written in column address 200h-3FFh of a flash memory one by one from buffer memory. This data is 512 bytes of data equivalent to one fourth of the sector capacity of a flash memory.
[0074] "FFh" which is dummy data is written in like time of day t1-t2 after time of day t3.

[0075] Drawing 14 is a wave form chart of operation for explaining in more detail the situation of the data transfer from the buffer memory shown in drawing 13 to a flash memory.
[0076] With reference to drawing 10 and drawing 14 , light-sector enable signal WSE** falls from H level to L level in time of day t0 according to the write-in demand from a host system. It responds and reset of a fall and the SC counter 26 is canceled for a reset signal RST of H level to L level. Moreover, the output enable input signal / OE** of buffer memory will be in a condition with accessible fall and buffer memory 4 from H level to L level.
[0077] In time of day t1-t2, the data out signal which a selector 34 outputs is written in a flash memory synchronizing with the start of clock signal SC. The counted value corresponding to the write-in column address at that time counts up with the SC counter 26. Since a media sector address (MA1, MA0) is not in agreement with 2 bits of high orders of the SC counter 26 in time of day t1-t2, data out signal DOs are fixed data "FFh" inputted into the input node by the side of "1" of a selector 34.
[0078] In time of day t2, according to change of counted value, the data of the address with which the comparison result signal CMP is specified as a fall and address signal ADR from H level to L level are read from buffer memory 4, and it is transmitted to a flash memory as a data out signal D0 through a selector 34. Data transfer is performed from buffer memory to a flash memory until it continues till time of day t3 henceforth.
[0079] After 512 bytes of data transfer of data 0h- data 1FFh is completed, in order that the comparison result signal CMP may start on H level from L level in time of day t3 according to change of counted value, a data out signal serves as a fixed value "FFh" inputted into the input node by the side of "1" of a selector 34 again.
[0080] As explained above, the store of the gestalt 1 of operation is used suitable for momentary preservation of an application which package elimination is carried out and adds data serially after that, for example, the image of a digital camera, preservation of the acoustic signal of a pocket mold digital audio device, etc.
[0081] And since capacity of the buffer memory which performs temporary data storage can be made small according to media sector capacity when the media sector capacity which is the unit capacity of data transfer with a host system is smaller than the capacity of 1 sector of the flash memory to be used, when hardware is constituted, the advantageous storage in cost can be offered.
[0082] [Gestalt 2 of operation] drawing 15 is the block diagram showing the outline configuration of the store 51 of the gestalt 2 of operation.
[0083] With reference to drawing 15 , it is for delivering and receiving the external data remembered to be a host system 12, a store 51 performs address translation in response to the media address from a host system, and in order to deliver and receive external data between host systems, it contains the data I/O section 59 which performs data conversion, and the flash memory 60 which performs data transfer according to the address signal which the data I/O section 59 changed. The data I/O section 59 changes the data between the data and external data which a flash memory 60 outputs and inputs.
[0084] The data I/O section 59 contains the flash plate interface section 57 of buffer memory 54 and a flash memory 60 which controls data transfer according to a host system 12, the host interface section 52 which performs data transfer, the buffer memory 54 which has the capacity of 512 bytes which stores stored data temporarily in order that the host interface section 52 may perform a host system 12 and data transfer, and the command from the host interface section 52.
[0085] The flash plate interface section 57 is the sequence united with the specification of a flash memory, and contains the column address control section 58 which generates the start column address which specifies the read-out starting position of a column specified by the sector address and sector address of a flash memory from the sequencer section 56 which sends out the address for specifying a memory area at the time of the command, read-out, and the store which set up actuation of read-out, a store, etc. to a flash memory, and the media sector address given from the host system 12.
[0086] In drawing 15 , a flash memory 60 has the division lead / program function which can carry out read-out and write-in initiation for a lead and program of data from the column address of the arbitration of a sector.
[0087] A flash memory 60 has two or more sectors with the capacity whose each is 2048 bytes. A flash memory can output the data of only the specified sector capacitive component serially synchronizing with a clock signal, if a sector address is specified. And if a start column address is specified further, even the data which correspond to the last address of a sector from the data applicable to the column address of the specified sector can be serially outputted synchronizing with a clock signal.
[0088] Drawing 16 is a memory map in which the response relation of the flash memory and buffer memory in the gestalt 2 of operation is shown.
[0089] Since the memory map shown in drawing 16 shows the same assignment as the memory map used for the gestalt 1 of operation shown in drawing 2 , explanation is not repeated.
[0090] Drawing 17 is drawing for explaining that a media sector address is changed into a flash plate sector address and a start column address.
[0091] With reference to drawing 17 , 14 bits of high orders of the media sector addresses MA15-MA0 are used as flash plate sector addresses SA13-SA0. Moreover, MA1 and MA0 which are 2 bits of low order among media sector addresses are used as CA10 and CA9 among start column addresses, respectively. Moreover, all of CA11, CA8-CA0 which are other bits of a start column address are set as "0h."
[0092] Drawing 18 is drawing showing 2 bits [of low order of the start column address of a flash memory, and a media sector address] relation.
[0093] With reference to drawing 18 , when both MA1 and MA0 are 0, a start column address is set as 0h, and when MA1 and MA0 are 0 and 1, respectively, a start column address is set as 200h.

[0094] When MA1 and MA0 are 1 and 0, respectively, a start column address is set as 400h, and when both MA1 and MA0 are 1, a start column address is set as 600h. Although this address translation is performed by the column address control section 58 of drawing 15 , it is easily realizable only by connecting wiring corresponding to drawing 1818 .
[0095] Drawing 19 is a conceptual diagram for explaining a start column address. With reference to drawing 19 , when 1 sector is 2048 bytes, the column address of 0h-7FFh exists corresponding to the flash plate sector address SA. Setting out of the start column address CA starts read-out synchronizing with a clock signal from the data of the column corresponding to the start column address in the set-up flash plate sector address SA.
[0096] Drawing 20 is a wave form chart of operation for explaining command setting out at the time of reading data from the flash memory which has a division lead / program function, and address selection.
[0097] If the start of a write enable signal / WE** is detected in time of day t1 with reference to drawing 20 when a command data enable signal / CDE** is L level, a lead command will be incorporated by the flash memory in the timing.
[0098] In time of day t2, SA (1) which is 8 bits of low order of a sector address is incorporated in the start edge of a write enable signal / WE**. Subsequently, in time of day t3, SA (2) which is 6 bits of high orders of a sector address is incorporated by the flash memory in the start edge of a write enable signal / WE**.
[0099] Subsequently, in time of day t4, CA (1) which is 8 bits of low order of the start column address CA with the start edge of a write enable signal / WE** is incorporated by the flash memory. Then, in time of day t5, CA (2) which is 4 bits of high orders of a start column address with the start edge of a write enable signal / WE** is incorporated.
[0100] After time of day t6, the data of the start column address specified from the address / data input/output terminal synchronizing with clock signal SC are made into a head, and data are outputted from a flash memory.
[0101] Drawing 21 is drawing showing the input wave which writes data in a flash memory in the gestalt 2 of operation.
[0102] A program command will be read into a flash memory, if the start edge of a write enable signal / WE** is detected in time of day t1 with reference to drawing 21 when command data enable input / CDE** is L level.
[0103] Then, in time of day t2, SA (1) which is 8 bits of low order of a sector address with the start edge of a write enable signal / WE** is incorporated by the flash memory. Then, in time of day t3, SA (2) which is 6 bits of high orders of a sector address with the start edge of a write enable signal / WE** is incorporated by the flash memory.
[0104] In time of day t4, CA (1) which is 8 bits of low order of a start column address with the start edge of a write enable signal / WE** is incorporated by the flash memory. Then, in time of day t5, CA (2) which is 4 bits of high orders of a start column address with the start edge of a write enable signal / WE** is incorporated by the flash memory. Address selection is completed above.
[0105] Data are written in the address which a data input is serially carried out synchronizing with clock signal SC, using the data corresponding to the start column address of the set-up sector address as a head after time of day t6, and corresponds.
[0106] Control which gives the command to the flash memory shown by drawing 20 and drawing 21 and an address signal is performed in the flash plate interface sequencer section 56 in drawing 15 R> 5.
[0107] Drawing 22 is drawing showing the Maine flow of processing of the storage of the gestalt 2 of operation. With reference to drawing 22 , the Maine flow of processing of the storage of the gestalt 2 of operation differs from the flow which the point which replaces with the read-out processing step S04 of the gestalt 1 of operation shown in drawing 5 , replaces with the write-in processing step S05 including step S104, and contains step S105 showed by drawing 5 . Since other parts are the same as that of the flow shown by drawing 5 , explanation is not repeated.
[0108] Drawing 23 is a flow chart which shows the detail of read-out processing of step S104 shown in drawing 22 .
[0109] With reference to drawing 23 , read-out is started in step S111. Subsequently, in step S112, a media sector address is received from a host system. Then, in step S113, the media sector address which received is changed and the sector address SA of a flash memory and the start column address CA are generated. Then, in step S114, the division lead command of a flash memory is set up and a sector address SA and the start column address CA are specified. And in step S115, data are read from a flash memory and written in buffer memory.
[0110] Termination of the store to buffer memory sends out an interrupt signal to a host system in step S116.
[0111] Then, in step S117, the data written in buffer memory are sent out as read-out data to a host system. And read-out is completed in step S118.
[0112] Drawing 24 is drawing showing with which block in a store each step of the read-out processing shown by drawing 23 is carried out.
[0113] With reference to drawing 24 , the read-out demand of a media sector address is first sent from a host system to a controller or buffer memory. A controller corresponds to the host interface section 52 and the flash plate interface sequencer section 56 in drawing 15 .
[0114] In response by the controller, the sector address SA of a flash memory and the start column address CA are generated from a media sector address. And from a controller, a lead command, a sector address, and a start column address are sent out to a flash memory. It responds, and in a flash memory, division lead actuation is performed and the data which are 512 bytes are outputted to buffer memory. After the data store to buffer memory is completed, a controller requires data read-out of the specified media sector address from a host system. And from buffer memory, read-out of data is performed to a host system, and read-out actuation is ended.
[0115] Drawing 25 is a flow chart which shows the detail of the write-in processing in step S105 shown in drawing 22 .
[0116] With reference to drawing 25 , a store is first started in step S121. Then, the media sector address sent from the host system in step S122 is received.

[0117] Then, in step S123, a store requires data from a host system. And in step S124, data are received from a host system. This data is written in buffer memory in step S125.
[0118] And in step S126, the sector address SA of a flash memory and the start column address CA are generated from the media sector address which received at step S122. Then, in step S127, a division program command is set up to a flash memory, and assignment of a sector address SA and the start column address CA is carried out continuously.
[0119] And in step S128, data are read from buffer memory and written in a flash memory. And the store of data is completed in step S129.
[0120] Drawing 26 is drawing showing how each step of the write-in processing shown in drawing 25 is performed between a host system, a controller and buffer memory, and a flash memory.
[0121] With reference to drawing 26 , the write-in demand of a media sector address is first sent towards a controller from a host system. Then, in response, a controller gives the data write-in demand of a media sector address to a host system. Responding, a host system writes in the data to a media sector address. This data is inputted into buffer memory via a controller.
[0122] Then, by the controller, the sector address SA of a flash memory and the start column address CA are generated from the media sector address which had received. And a controller performs setting out of a program command, a sector address/SA, and a start column address / CA to a flash memory. Responding, a flash memory performs division program actuation. And from a buffer, 512 bytes of data are inputted to a flash memory, a predetermined column address is made into a head, and a data store is performed. If 512 bytes of write data is inputted into a flash memory from buffer memory, the predetermined store after weight time amount progress will be completed after that.
[0123] In the gestalt 2 of operation, generation of the address signal given to a flash memory from address control and the media sector address of buffer memory is performed by the column address control section 58 in drawing 15 .
[0124] Drawing 27 is the block diagram showing the detail of the column address control section 58 in drawing 15 .
[0125] Drawing 27 is referred to. The column address control section 58 The flip-flop 72 which latches lead sector enable signal RSE** generated inside a store synchronizing with the start of clock signal SC, AND circuit 74 which outputs the OR of the output of a flip-flop 72, and light-sector enable signal WSE** generated inside a store as a reset signal RST, The 9-bit SC counter 76 which is reset by the reset signal RST, answers the start of clock signal SC after that, and starts count-up, A 16-bit media sector address is latched from a host system. 14 bits of high orders, The media sector-address latch section 30 which outputs 2 bits of low order to the sequencer section 6 as sector addresses SA0-SA15 and start column addresses 0-CAs 1, respectively, The gate circuit 78 which outputs a write enable signal / WE** in response to the output and clock signal SC of a flip-flop 72 is included.
[0126] In addition, buffer memory 4 is indicated by drawing 10 for the facilities of explanation. Buffer memory 4 receives the enumerated data of 9 bits of the SC counter 26 as address signal ADR, receives light-sector enable signal WSE** as an output enable signal /OE**, undergoes the output of a gate circuit 28 as a write enable signal /WE**, answers these, and is held in response to data input DI from a flash memory, or sends out data output DO to a flash memory.
[0127] Since capacity of the buffer memory which stores data temporarily can be made smaller than the capacity of 1 sector of a flash memory in the gestalt 2 of operation when the host interface section performs a host system and data transfer as explained above, storage with a cost merit can be offered. Furthermore, read-out and rewrting are possible per media sector by using it, carrying a division lead / programmable flash memory.
[0128] It should be thought that the gestalt of the operation indicated this time is [no] instantiation at points, and restrictive. The range of this invention is shown by the above-mentioned not explanation but claim, and it is meant that all modification in a claim, equal semantics, and within the limits is included.
[0129]
[Effect of the Invention] Since the storage which carries a flash memory according to claim 1 carries the buffer memory of smallness capacity when using the flash memory which carries out sector read-out as a semiconductor device for storage, it is advantageous in cost.
[0130] In order that the storage which carries a flash memory according to claim 2 may write in the same data as the data immediately after eliminating a flash memory as dummy data in addition to the effectiveness that the storage which carries a flash memory according to claim 1 does so, the data of a part with which data-hold was already performed are not lost.
[0131] In addition to the effectiveness that the storage which carries a flash memory according to claim 1 does so, the sector capacity of a flash memory can be divided and used for the storage which carries a flash memory according to claim 3 to 5 by external media sector capacity, and a flash memory can be efficiently used for it.
[0132] In addition to the effectiveness that the storage which carries a flash memory according to claim 1 does so, also in case the storage which carries a flash memory according to claim 6 to 7 reads sector data, the buffer memory of small capacity can be used for it.
[0133] In addition to the effectiveness that the storage which carries a flash memory according to claim 6 does so, the sector capacity of a flash memory can be divided and used for the storage which carries a flash memory according to claim 8 to 10 by external media sector capacity, and a flash memory can be efficiently used for it.
[0134] Since the store which carries a flash memory according to claim 11 to 12 carries the buffer memory of small capacity, it is advantageous in cost, and rewrting of data is still more possible for it per media sector.

[Translation done.]

TECHNICAL FIELD

[Field of the Invention] More specifically, this invention relates to the storage which carries a flash memory about storage.

[Translation done.]

* NOTICES *

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2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

PRIOR ART

[Description of the Prior Art] In recent years, the storage capacity of a flash memory is also becoming large with the advance of a semi-conductor manufacturing technology. With this large-capacity-izing, it is small and the storage which carried the flash memory as an archive medium in the field of a pocket device especially taking advantage of the property which is a low power has come to be used.

[Translation done.]

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EFFECT OF THE INVENTION

[Effect of the Invention] Since the storage which carries a flash memory according to claim 1 carries the buffer memory of smallness capacity when using the flash memory which carries out sector read-out as a semiconductor device for storage, it is advantageous in cost.
[0130] In order that the storage which carries a flash memory according to claim 2 may write in the same data as the data immediately after eliminating a flash memory as dummy data in addition to the effectiveness that the storage which carries a flash memory according to claim 1 does so, the data of a part with which data-hold was already performed are not lost.
[0131] In addition to the effectiveness that the storage which carries a flash memory according to claim 1 does so, the sector capacity of a flash memory can be divided and used for the storage which carries a flash memory according to claim 3 to 5 by external media sector capacity, and a flash memory can be efficiently used for it.
[0132] In addition to the effectiveness that the storage which carries a flash memory according to claim 1 does so, also in case the storage which carries a flash memory according to claim 6 to 7 reads sector data, the buffer memory of small capacity can be used for it.
[0133] In addition to the effectiveness that the storage which carries a flash memory according to claim 6 does so, the sector capacity of a flash memory can be divided and used for the storage which carries a flash memory according to claim 8 to 10 by external media sector capacity, and a flash memory can be efficiently used for it.
[0134] Since the store which carries a flash memory according to claim 11 to 12 carries the buffer memory of small capacity, it is advantageous in cost, and rewrting of data is still more possible for it per media sector.

[Translation done.]

TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] A flash memory is nonvolatile and is the semiconductor memory which can perform rewrting after package elimination. In order to accumulate a storage element on high density and to carry out data transfer to a high speed, a sector address is specified, per sector, the data of a constant rate are put in block and, as for a flash memory, read-out, elimination, and a store (program) are performed for them. Being [for example,] in the inclination which the sector capacity which is the unit as for which a flash memory reads data collectively also increases with large-capacity-izing of a flash memory, by the 256M bit AND mold flash memory, this sector capacity has become 2048 bytes.
[0004] the data volume (in this description, media sector capacity is called henceforth) of the unit at the time of on the other hand the information machines and equipment which make a personal computer the start performing data transfer with stores, such as a hard disk and a memory card, -- for example, it is 512 bytes standardly and the inclination which especially this media sector capacity increases is not seen.
[0005] It is necessary to store the sector data of a flash memory temporarily and to carry the buffer memory for performing timing for performing data transfer with a host system, and adjustment of capacity in the interior of a store in the store which carries such a flash memory with a sector structure. As for this buffer memory, SRAM (Static Random Access Memory) etc. is usually used.
[0006] Rather than the sector capacity of a flash memory, even when it was small capacity, the capacity, i.e., the media sector capacity, of data transfer with a host system, it needed to make capacity of buffer memory the sector capacity of a flash memory, this capacity, or the capacity beyond it.
[0007] However, the sector capacity of a flash memory had large-capacity-ized every year, in such a case, mass SRAM needed to be carried as buffer memory, and the demerit had arisen in cost in it.
[0008] It is offering the storage which carries the flash memory which this invention's was made as [solve / such a trouble], and the object's made it possible to carry the buffer memory of the small capacity equivalent to media sector capacity, and aimed at the cost cut.

[Translation done.]

* NOTICES *

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MEANS

[Means for Solving the Problem] The storage which carries a flash memory according to claim 1 It is storage equipped with the write-in mode in which data storage is performed in response to an external write-address signal and an external write data from a host system. Package elimination which makes a smallest unit the memory area holding the data of a predetermined number at the time of data elimination is performed. It has the flash memory by which the store of two or more data is made by making the data length of a predetermined number into a unit. A flash memory In write-in mode, incorporate and hold two or more data contained in an internal write data in response to an internal write-address signal, and it sets in write-in mode. It has further the data I/O section which generates an internal write-address signal in response to an external write-address signal, holds in response to an external write data, and outputs an internal write data based on an external write data and an external write-address signal. The data I/O sections are the 1st interface section which receives an external write data and an external write-address signal from a host system in write-in mode, and more than the number of external write datas. And it sets in the buffer memory which has memory capacity smaller than the number of internal write datas, and receives an external write data from the 1st interface section in write-in mode, and write-in mode. In response to an external write-address signal, an internal write-address signal is generated from the 1st interface section. The 2nd interface section which adds the dummy data corresponding to the external write-address signal which data rewriting of a memory area does not produce in the external write data read from buffer memory, and generates an internal write data is included.
[0010] The storage which carries a flash memory according to claim 2 In the configuration of the store which carries a flash memory according to claim 1 dummy data It is a value corresponding to the data held immediately after carrying out data elimination of the flash memory. The 2nd interface section Outputting serially the data of the data length contained in an internal write data in predetermined sequence, an external write data occupies the continuous location which makes a head location the location corresponding to an external write-address signal in predetermined sequence.
[0011] The storage which carries a flash memory according to claim 3 makes a unit the number of data by which a head location is included in an external write data in the configuration of the storage which carries a flash memory according to claim 2 according to an external write-address signal, and it is discontinuously determined on the basis of [of predetermined sequence] the 1st.
[0012] The number of data by which the storage which carries a flash memory according to claim 4 is contained in an internal write data in the configuration of the storage which carries a flash memory according to claim 3 is the integral multiple of the number of data contained in an external write data.
[0013] The storage which carries a flash memory according to claim 5 In the configuration of the storage which carries a flash memory according to claim 2, in addition, a flash memory Synchronizing with a clock, an internal write data is incorporated one by one. The 2nd interface section Generate the read-out control signal over buffer memory, and an internal write data is generated in response to an external write data from buffer memory. It has the data transfer control section which generates an internal write-address signal from an external write-address signal. A data transfer control section The counter which starts the count of a clock when the store of an internal write data is started by the flash memory, The comparator which outputs a coincidence signal when a predetermined number bit is in agreement from the high order of the counted value of the offset signal included in an external write-address signal, and a counter, The gate circuit which gives a read-out control signal to buffer memory according to a coincidence signal so that buffer memory may output an external write data synchronizing with a clock, When the coincidence signal is deactivated, the value corresponding to the initial value after elimination of a flash memory is given to a flash memory, and when a coincidence signal is activated, it has the selection circuitry which gives the external write data read from buffer memory to a flash memory.
[0014] The storage which carries a flash memory according to claim 6 It adds to the configuration of the storage which carries a flash memory according to claim 1. It has further the read-out mode which outputs external read-out data to a host system in response to an external read-out address signal from a host system. The data I/O section At the time of read-out mode, in response to an external read-out address signal, generate an internal read-out address signal, and it gives a flash memory. After choosing some internal read-out data read from a flash memory and holding as external read-out data, External read-out data are outputted to a host system. The 1st interface section At the time of read-out mode, the external read-out data according to a carrier beam external read-out address signal are outputted to a host system from a host system. Buffer memory Are more than the number of external read-out data, and it has storage capacity smaller than the number of internal read-out data. The external read-out data currently held to the 1st interface section at the time of read-out mode are

outputted. The 2nd interface section Two or more data which generate an internal read-out address signal in response to an external read-out address signal from the 1st interface section, give to a flash memory, and internal read-out data contain from a flash memory at the time of read-out mode Read-out, It sends out to buffer memory by using some internal read-out data as external read-out data.

[0015] In addition to the configuration of the storage with which the storage which carries a flash memory according to claim 7 carries a flash memory according to claim 6, a flash memory outputs serially the data of the data length contained in internal read-out data according to an internal read-out address signal in predetermined sequence, and external read-out data occupy the continuous location which makes a head location the location corresponding to an external read-out address signal in predetermined sequence.

[0016] In the configuration of the storage with which the storage which carries a flash memory according to claim 8 carries a flash memory according to claim 7, a head location is discontinuously determined on the basis of [of predetermined sequence] the 1st by making into a unit the number of data contained in external read-out data according to an external read-out address signal.

[0017] The number of data by which the storage which carries a flash memory according to claim 9 is contained in an internal write data in the configuration of the storage which carries a flash memory according to claim 8 is the integral multiple of the number of data contained in an external write data.

[0018] The storage which carries a flash memory according to claim 10 In the configuration of the storage which carries a flash memory according to claim 7, in addition, a flash memory Synchronizing with a clock, the sequential output of the internal read-out data is carried out. The 2nd interface section Generate an internal read-out address signal from an external read-out address signal, and generate a write control signal to buffer memory so that some internal read-out data may be chosen and buffer memory may store as external read-out data. It has a data transfer control section. A data transfer control section The counter which starts the count of a clock when read-out of internal read-out data is started from a flash memory, The comparator which outputs a coincidence signal when a predetermined number bit is in agreement from the high order of the counted value of the offset signal included in an external write-address signal, and a counter, It has the gate circuit which gives a write control signal to buffer memory according to a coincidence signal so that buffer memory may store some internal read-out data as external read-out data synchronizing with a clock.

[0019] The storage which carries a flash memory according to claim 11 The data I/O section which generates the internal main address corresponding to [are the storage which performs data storage which delivers and receives external data in response to an external address signal from a host system, and] the external address, and the internal secondary address, Package elimination which makes a smallest unit the memory area holding the data of a predetermined number at the time of data elimination is performed. Selection of a memory area unit is performed by the internal main address, and it has the flash memory which can deliver and receive serially the in-house data which the data transfer starting position in a memory area is specified, and contains two or more data with the internal secondary address. The memory capacity of a memory area is larger than the number of data contained in external data, and the internal secondary address is discontinuously generated on the basis of the start address of a memory area by making into a unit the number of data contained in an external write data.

[0020] In addition to the configuration of the storage with which the storage which carries a flash memory according to claim 12 carries a flash memory according to claim 11, the data I/O section contains the buffer memory which has the memory capacity corresponding to the number of data contained in the external data which hold external data and an in-house data temporarily, in order to carry out timing adjustment between a host system and a flash memory.

[0021]

[Embodiment of the Invention] The gestalt of operation of this invention is explained in detail, referring to a drawing below. In addition, a same-among drawing sign shows the same or a considerable part.

[0022] [Gestalt 1 of operation] drawing 1 is the block diagram showing the outline configuration of the store 1 which carried the flash memory.

[0023] With reference to drawing 1 , it is for delivering and receiving the external data remembered to be a host system 12, a store 1 performs address translation in response to the media address from a host system, and in order to deliver and receive external data between host systems, it contains the data I/O section 9 which performs data conversion, and the flash memory 10 which performs data transfer according to the address signal which the data I/O section 9 changed. The data I/O section 9 changes the data between the data and external data which a flash memory 10 outputs and inputs.

[0024] The data I/O section 9 contains a host system, the host interface section 2 which performs data transfer, the buffer memory 4 which has the capacity of 512 bytes which stores some sector data of a flash memory temporarily in order that the host interface section 2 may perform a host system 12 and data transfer, the flash plate interface section 7 which controls data transfer with buffer memory 4 and a flash memory according to the command from the host interface section 2, and the flash memory 10 which is a semiconductor device holding the data which a store 1 should memorize.

[0025] The flash plate interface section 7 is the sequence united with the specification of a flash memory, and contains the data transfer control section 8 which generates the sector address of a flash memory, and column address offset from the sequencer section 6 which sends out the address for specifying a memory area at the time of the command, read-out, and the store which set up actuation of read-out, a store, etc. to a flash memory, and the media sector address given from the host system 12.

[0026] A flash memory 10 has two or more sectors with the capacity whose each is 2048 bytes. A flash memory 10 can output serially 2048 bytes of data memorized by the specified sector, if a sector address is specified.

[0027] Drawing 2 is a memory map in which the response relation of the address of the flash memory and buffer memory in the gestalt 1 of operation is shown.
[0028] With reference to drawing 2 , 512 bytes and 1 sector of a flash memory 10 are the memory rises in the case of being 2048 bytes, and media sector capacity, i.e., the sector capacity which performs [a store 1] data transfer collectively, is assigning 1/4 sector of a flash memory 10 as a media sector.
[0029] For example, it is equivalent to flash plate sector-address 0h flash plate column address 0h-1FFh media sector-address 0h. Media sector-address 1h, it is equivalent to flash plate sector-address 0h flash plate column address 200h-3FFh. Similarly, it is equivalent to flash plate sector-address 0h flash plate column address 400h-5FFh media sector-address 2h. Media sector-address 3h, it is equivalent to flash plate sector-address 0h flash plate column address 600h-7FFh. That is, each flash plate sector address is quadrisected, respectively, and is assigned to the media sector address.
[0030] Drawing 3 is drawing for giving explanation which changes a media sector address into a flash plate sector address and a column address offset generation bit.
[0031] With reference to drawing 3 , 14 bits of high orders of the media sector addresses MA15-MA0 are used as flash plate sector addresses SA13-SA0. Moreover, MA1 and MA0 which are 2 bits of low order among media sector addresses are used as column address offset generation bits C1 and C0, and it generates the start flash plate column address offset later explained from this column address offset generation bit.
[0032] Drawing 4 is drawing showing 2 bits [of low order of start flash plate column address offset and a media sector address] relation.
[0033] With reference to drawing 4 , when both MA1 and MA0 are 0, start flash plate column address offset is set as 0h, and transfer of 512 bytes of data which are media sector capacity is performed between buffer memory and a flash memory.
[0034] When MA1 and MA0 are 0 and 1, respectively, start flash plate column address offset is set as 200h, and data transfer between buffer memory and a flash memory is performed.
[0035] When MA1 and MA0 are 1 and 0, respectively, start flash plate column address offset is set as 400h, and data transfer is performed between buffer memory and a flash memory.
[0036] When both MA1 and MA0 are 1, start flash plate column address offset is set as 600h, and data transfer between buffer memory and a flash memory is performed.
[0037] Drawing 5 is drawing showing the Maine flow of processing of the storage of the gestalt 1 of operation. With reference to drawing 5 , step S01 is a step of the waiting for the demand from a host system. Then, it is judged in step S02 whether there was any demand of read-out. When there is a read-out demand, it moves to step S04 and read-out processing is performed. If read-out processing is completed, it will be in the state waiting for a demand from a return host system to step S01 again.
[0038] In step S02, when the read-out demand is not performed, it progresses to step S03. At step S03, it is judged whether the write-in demand is performed from the host system. When there is a write-in demand, it progresses to step S05 and write-in processing is performed. If write-in processing is completed, again, it progresses to step S01 and will be in the state waiting for a demand from a host system.
[0039] In step 03, when a write-in demand is not performed, it will be in return and the state waiting for a demand from a host system to step S01 again.
[0040] Drawing 6 is a flow chart which shows the detail of read-out processing of step S04 shown in drawing 5 .
[0041] With reference to drawing 6 , read-out is started in step S11. Subsequently, in step S12, a media sector address is received from a host system. Then, address translation is performed based on the media sector address which received, and the value of the start flash plate column address offset shown by drawing 4 is generated.
[0042] Then, in step S14, sector read-out is performed from a flash memory. And the read data are written in buffer memory in step S15 based on an offset value. Then, in step S16, an interrupt signal is sent out to a host system and the data written in buffer memory are sent out as read-out data to a host system in step S17. And read-out is completed in step S18.
[0043] Drawing 7 is drawing showing with which block in a store each step of the read-out processing shown in drawing 6 is carried out.
[0044] With reference to drawing 7 , the read-out demand of a media sector address is first sent from a host system to a controller or buffer memory. A controller corresponds to the host interface section 2 and the flash plate interface sequencer section 6 in drawing 1 .
[0045] In response by the controller, generation of an offset value is considered as the sector address SA of a flash memory from a media sector address. And a lead command and a sector address SA are sent to a flash memory. It responds, and in a flash memory, a sector lead is performed and the data which are 2048 bytes are sent out to a controller as flash plate interface data output one by one. In response, by the controller, 512 bytes of data corresponding to the offset based on a media sector address are extracted, and it transmits to buffer memory.
[0046] And after storing of the data to buffer memory is completed, a controller performs the data read-out demand of a media sector address to a host system, and a host system receives interruption. Then, a controller outputs data from buffer memory and, thereby, data read-out of a media sector address is performed. And read-out is completed.
[0047] Drawing 8 is a flow chart which shows the detail of the write-in processing in step S05 shown in drawing 5 .
[0048] With reference to drawing 8 , a store is first started in step S21. Then, the media sector address sent from the host system in step S22 is received.
[0049] Then, in step S23, a store requires data from a host system. And in step S24, a store receives data from a host system.

This data is written in buffer memory in step S25.
[0050] And in step S26, generation of an offset value is carried out from the media sector address which received at step S22. Then, in step S27, setting out of the program command to a flash memory is carried out. Then, in step S28, the data from buffer memory are compounded with initial value data, and a store is performed to a flash memory to predetermined timing.
[0051] And a store is completed in step S29. Drawing 9 is drawing showing how each step of the write-in processing shown in drawing 8 is performed between a host system, a controller and buffer memory, and a flash memory.
[0052] With reference to drawing 9 , the write-in demand of a media sector address is first sent towards a controller from a host system. Then, in response, a controller gives the data write-in demand to a media sector address to a host system. Responding, a host system writes in the data to a media sector address. This data is inputted into buffer memory via a controller.
[0053] Then, by the controller, generation of the sector address of a flash memory and an offset value is carried out from the media sector address which had received. And dispatch of the program command and sector address to a flash memory is carried out.
[0054] In response, a flash memory will be in the condition which can be data written in. And based on the predetermined signal of a controller, 512 bytes of data stored based on the offset value are transmitted from buffer memory. "FFh" is transmitted as write datas other than the period when the data stored in buffer memory among the periods when the write data to a flash memory is transmitted are transmitted. If the write data containing the data of buffer memory is inputted into a flash memory, the predetermined store after weight time amount progress will be completed after that.
[0055] Here, write-in data "FFh" are explained. Each memory cell of a flash memory consists of MOS transistors which have the floating gate. Each memory cell holds data "1" and "0" in the state of the threshold electrical potential difference of an MOS transistor. Generally, the condition immediately after elimination of a memory cell corresponds to maintenance data "1." If write-in actuation of data "0" is carried out, a threshold electrical potential difference will change, and the condition of a memory cell of having a threshold electrical potential difference after change corresponds to maintenance data "0." On the other hand, a threshold electrical potential difference does not change in write-in actuation of data "1." For this reason, even if write-in actuation of data "1" is performed to the memory cell which holds data "0" as an initial state, maintenance data do not change.
[0056] That is, although the store of data is usually performed after elimination of memory cell data is performed, with the gestalt 1 of operation, elimination actuation is not performed but "FFh" is written in as data. Since "FFh" is data all whose bits are 1 byte of "1", a flash memory holds data just before writing in.
[0057] Drawing 10 is the block diagram showing the detail of the data transfer control section 8 shown in drawing 1 . The flip-flop 22 which latches lead sector enable signal RSE** by which the data transfer control section 8 is generated inside a store with reference to drawing 10 synchronizing with the start of clock signal SC, AND circuit 24 which outputs the OR of the output of a flip-flop 22, and light-sector enable signal WSE** generated inside a store as a reset signal RST, The SC counter 26 which is reset by the reset signal RST, answers the start of clock signal SC after that, and starts count-up, The media sector-address latch section 30 which latches a 16-bit media sector address and outputs 14 bits of high orders to the sequencer section 6 as sector addresses SA0-SA15 from a host system, The comparator 32 which compares 2 bits of high orders with 2 bits of low order of the media sector address which the media sector-address latch section 30 latched among the enumerated data of 11 bits which are the outputs of the SC counter 26 is included.
[0058] A comparator 32 outputs CMP for the comparison result signal used as L level, when the 2 bits data from the SC counter 26 and the 2-bit data from the media sector-address latch section 30 are in agreement.
[0059] The data transfer control section 8 contains further the output of a flip-flop 22, clock signal SC, the gate circuit 28 that outputs a write enable signal / WE** in response to Signal CMP a result, and the output from buffer memory 4 and the selector 34 outputted to a flash memory according to the comparison result signal CMP in response to fixed data "FFh." A selector 34 outputs the output from buffer memory to a flash memory, when the comparison signal CMP is L, and when the comparison signal CMP is H, it outputs fixed data "FFh" to a flash memory.
[0060] In addition, buffer memory 4 is indicated by drawing 10 for the facilities of explanation. Buffer memory 4 receives 9 bits of low order of the enumerated data of 11 bits of the SC counter 26 as address signal ADR, receives light-sector enable signal WSE** as an output enable signal /OE**, undergoes the output of a gate circuit 28 as a write enable signal /WE**, answers these, and is held in response to data input DI from a flash memory, or sends out data output DO to a flash memory through a selector 34.
[0061] Drawing 11 is the timing chart showing the situation of the data transfer from a flash memory to buffer memory.
[0062] With reference to drawing 11 , data signal DATA is read from a flash memory according to time of day t1 to clock signal SC. Since it is carried out per sector, this read-out is read after 2048 data usually continue.
[0063] the least significant 2 bits among the media sector addresses specified from the host system here -- it is (MA1, MA0) -- when it is (0, 1), in time of day t1-t2, the data read from the flash memory are not transmitted to buffer memory.
[0064] And in time of day t2-t3, while the data equivalent to column address 200h-3FFh are read from the flash memory, these data are transmitted to buffer memory and held. This data held is 512 bytes of 2048-byte sector capacity read from a flash memory, and is the quadrant of sector capacity.
[0065] Although the data after column address 400h are read after time of day t3 one by one, these are not held to buffer memory.
[0066] Drawing 12 is the wave form chart of operation having shown more actuation of the data store to the buffer memory

shown in drawing 11 in the detail.
[0067] With reference to drawing 10 and drawing 12 , lead sector enable signal RSE** falls from H level to L level in time of day t0 according to the read-out demand having been performed from the host system. Then, in time of day t1, reset of a fall and the SC counter 26 is canceled for a reset signal RST of H level to L level. Henceforth, in time of day t1-t2, the SC counter 26 counts up the counted value of 11 bits from 0h to 1FFh according to the input of clock signal SC. Address signal ADR inputted into the buffer memory which is 9 bits of low order of counted value changes from 0h to 1FFh similarly. Since 2 bits of high orders of the counted value inputted into a comparator 32 at this time are (0, 0) and the 2-bit inputs from the media sector-address latch section 30 are (0, 1), the comparison result signal CMP is H level which shows an inequality. Therefore, the content of data in signal DI is not written in buffer memory 4 in time of day t1-t2.
[0068] In time of day t2, the counted value of the SC counter 26 is set to 200h, and 2 bits of high orders of counted value are in agreement with the 2-bit signal inputted from the media sector-address latch section 30. It responds and the comparison result signal CMP falls from H to L level. namely, -- and the comparison result signal CMP serves as L level, while counted value is 200h-3FFh. According to change of this comparison result signal CMP, a gate circuit 28 makes clock signal SC a write enable signal /WE**, and outputs to buffer memory. Data 0h- data 1FFh which is a data input is written in the address with which address signal ADR in the start edge of a write enable signal / WE** shows buffer memory 4 since a write enable signal / WE** is inputted.
[0069] Since the counted value of the SC counter 26 is set to 400h or more after time of day t3, the comparison result signal CMP is again set to H level, and the data inputted henceforth are not written in buffer memory.
[0070] Drawing 13 is the timing chart showing the situation of the data transfer from buffer memory to a flash memory.
[0071] With reference to drawing 13 , when media sector addresses (MA1, MA0) are (0, 1), in time of day t1-t2, "FFh" which is dummy data is written in column address 0h-1FFh of a flash memory. This dummy data is data corresponding to the initial value immediately after elimination of a flash memory, and generally, even if a flash memory performs actuation which writes in this initial value data, the data already held inside are not destroyed.
[0072] Therefore, the store of the gestalt 1 of operation is used suitable for momentary preservation of an application which package elimination is carried out and adds data serially after that, for example, the image of a digital camera, preservation of the acoustic signal of a pocket mold digital audio device, etc.
[0073] In time of day t2-t3, data are written in column address 200h-3FFh of a flash memory one by one from buffer memory. This data is 512 bytes of data equivalent to one fourth of the sector capacity of a flash memory.
[0074] "FFh" which is dummy data is written in like time of day t1-t2 after time of day t3.
[0075] Drawing 14 is a wave form chart of operation for explaining in more detail the situation of the data transfer from the buffer memory shown in drawing 13 to a flash memory.
[0076] With reference to drawing 10 and drawing 14 , light-sector enable signal WSE** falls from H level to L level in time of day t0 according to the write-in demand from a host system. It responds and reset of a fall and the SC counter 26 is canceled for a reset signal RST of H level to L level. Moreover, the output enable input signal / OE** of buffer memory will be in a condition with accessible fall and buffer memory 4 from H level to L level.
[0077] In time of day t1-t2, the data out signal which a selector 34 outputs is written in a flash memory synchronizing with the start of clock signal SC. The counted value corresponding to the write-in column address at that time counts up with the SC counter 26. Since a media sector address (MA1, MA0) is not in agreement with 2 bits of high orders of the SC counter 26 in time of day t1-t2, data out signal DOs are fixed data "FFh" inputted into the input node by the side of "1" of a selector 34.
[0078] In time of day t2, according to change of counted value, the data of the address with which the comparison result signal CMP is specified as a fall and address signal ADR from H level to L level are read from buffer memory 4, and it is transmitted to a flash memory as a data out signal D0 through a selector 34. Data transfer is performed from buffer memory to a flash memory until it continues till time of day t3 henceforth.
[0079] After 512 bytes of data transfer of data 0h- data 1FFh is completed, in order that the comparison result signal CMP may start on H level from L level in time of day t3 according to change of counted value, a data out signal serves as a fixed value "FFh" inputted into the input node by the side of "1" of a selector 34 again.
[0080] As explained above, the store of the gestalt 1 of operation is used suitable for momentary preservation of an application which package elimination is carried out and adds data serially after that, for example, the image of a digital camera, preservation of the acoustic signal of a pocket mold digital audio device, etc.
[0081] And since capacity of the buffer memory which performs temporary data storage can be made small according to media sector capacity when the media sector capacity which is the unit capacity of data transfer with a host system is smaller than the capacity of 1 sector of the flash memory to be used, when hardware is constituted, the advantageous storage in cost can be offered.
[0082] [Gestalt 2 of operation] drawing 15 is the block diagram showing the outline configuration of the store 51 of the gestalt 2 of operation.
[0083] With reference to drawing 15 , it is for delivering and receiving the external data remembered to be a host system 12, a store 51 performs address translation in response to the media address from a host system, and in order to deliver and receive external data between host systems, it contains the data I/O section 59 which performs data conversion, and the flash memory 60 which performs data transfer according to the address signal which the data I/O section 59 changed. The data I/O section 59 changes the data between the data and external data which a flash memory 60 outputs and inputs.
[0084] The data I/O section 59 contains the flash plate interface section 57 of buffer memory 54 and a flash memory 60

which controls data transfer according to a host system 12, the host interface section 52 which performs data transfer, the buffer memory 54 which has the capacity of 512 bytes which stores stored data temporarily in order that the host interface section 52 may perform a host system 12 and data transfer, and the command from the host interface section 52.
[0085] The flash plate interface section 57 is the sequence united with the specification of a flash memory, and contains the column address control section 58 which generates the start column address which specifies the read-out starting position of a column specified by the sector address and sector address of a flash memory from the sequencer section 56 which sends out the address for specifying a memory area at the time of the command, read-out, and the store which set up actuation of read-out, a store, etc. to a flash memory, and the media sector address given from the host system 12.
[0086] In drawing 15 , a flash memory 60 has the division lead / program function which can carry out read-out and write-in initiation for a lead and program of data from the column address of the arbitration of a sector.
[0087] A flash memory 60 has two or more sectors with the capacity whose each is 2048 bytes. A flash memory can output the data of only the specified sector capacitive component serially synchronizing with a clock signal, if a sector address is specified. And if a start column address is specified further, even the data which correspond to the last address of a sector from the data applicable to the column address of the specified sector can be serially outputted synchronizing with a clock signal.
[0088] Drawing 16 is a memory map in which the response relation of the flash memory and buffer memory in the gestalt 2 of operation is shown.
[0089] Since the memory map shown in drawing 16 shows the same assignment as the memory map used for the gestalt 1 of operation shown in drawing 2 , explanation is not repeated.
[0090] Drawing 17 is drawing for explaining that a media sector address is changed into a flash plate sector address and a start column address.
[0091] With reference to drawing 17 , 14 bits of high orders of the media sector addresses MA15-MA0 are used as flash plate sector addresses SA13-SA0. Moreover, MA1 and MA0 which are 2 bits of low order among media sector addresses are used as CA10 and CA9 among start column addresses, respectively. Moreover, all of CA11, CA8-CA0 which are other bits of a start column address are set as "0h."
[0092] Drawing 18 is drawing showing 2 bits [of low order of the start column address of a flash memory, and a media sector address] relation.
[0093] With reference to drawing 18 , when both MA1 and MA0 are 0, a start column address is set as 0h, and when MA1 and MA0 are 0 and 1, respectively, a start column address is set as 200h.
[0094] When MA1 and MA0 are 1 and 0, respectively, a start column address is set as 400h, and when both MA1 and MA0 are 1, a start column address is set as 600h. Although this address translation is performed by the column address control section 58 of drawing 15 , it is easily realizable only by connecting wiring corresponding to drawing 1818 .
[0095] Drawing 19 is a conceptual diagram for explaining a start column address. With reference to drawing 19 , when 1 sector is 2048 bytes, the column address of 0h-7FFh exists corresponding to the flash plate sector address SA. Setting out of the start column address CA starts read-out synchronizing with a clock signal from the data of the column corresponding to the start column address in the set-up flash plate sector address SA.
[0096] Drawing 20 is a wave form chart of operation for explaining command setting out at the time of reading data from the flash memory which has a division lead / program function, and address selection.
[0097] If the start of a write enable signal / WE** is detected in time of day t1 with reference to drawing 20 when a command data enable signal / CDE** is L level, a lead command will be incorporated by the flash memory in the timing.
[0098] In time of day t2, SA (1) which is 8 bits of low order of a sector address is incorporated in the start edge of a write enable signal / WE**. Subsequently, in time of day t3, SA (2) which is 6 bits of high orders of a sector address is incorporated by the flash memory in the start edge of a write enable signal / WE**.
[0099] Subsequently, in time of day t4, CA (1) which is 8 bits of low order of the start column address CA with the start edge of a write enable signal / WE** is incorporated by the flash memory. Then, in time of day t5, CA (2) which is 4 bits of high orders of a start column address with the start edge of a write enable signal / WE** is incorporated.
[0100] After time of day t6, the data of the start column address specified from the address / data input/output terminal synchronizing with clock signal SC are made into a head, and data are outputted from a flash memory.
[0101] Drawing 21 is drawing showing the input wave which writes data in a flash memory in the gestalt 2 of operation.
[0102] A program command will be read into a flash memory, if the start edge of a write enable signal / WE** is detected in time of day t1 with reference to drawing 21 when command data enable input / CDE** is L level.
[0103] Then, in time of day t2, SA (1) which is 8 bits of low order of a sector address with the start edge of a write enable signal / WE** is incorporated by the flash memory. Then, in time of day t3, SA (2) which is 6 bits of high orders of a sector address with the start edge of a write enable signal / WE** is incorporated by the flash memory.
[0104] In time of day t4, CA (1) which is 8 bits of low order of a start column address with the start edge of a write enable signal / WE** is incorporated by the flash memory. Then, in time of day t5, CA (2) which is 4 bits of high orders of a start column address with the start edge of a write enable signal / WE** is incorporated by the flash memory. Address selection is completed above.
[0105] Data are written in the address which a data input is serially carried out synchronizing with clock signal SC, using the data corresponding to the start column address of the set-up sector address as a head after time of day t6, and corresponds.
[0106] Control which gives the command to the flash memory shown by drawing 20 and drawing 21 and an address signal is

performed in the flash plate interface sequencer section 56 in drawing 15 R> 5.
[0107] Drawing 22 is drawing showing the Maine flow of processing of the storage of the gestalt 2 of operation. With reference to drawing 22 , the Maine flow of processing of the storage of the gestalt 2 of operation differs from the flow which the point which replaces with the read-out processing step S04 of the gestalt 1 of operation shown in drawing 5 , replaces with the write-in processing step S05 including step S104, and contains step S105 showed by drawing 5 . Since other parts are the same as that of the flow shown by drawing 5 , explanation is not repeated.
[0108] Drawing 23 is a flow chart which shows the detail of read-out processing of step S104 shown in drawing 22 .
[0109] With reference to drawing 23 , read-out is started in step S111. Subsequently, in step S112, a media sector address is received from a host system. Then, in step S113, the media sector address which received is changed and the sector address SA of a flash memory and the start column address CA are generated. Then, in step S114, the division lead command of a flash memory is set up and a sector address SA and the start column address CA are specified. And in step S115, data are read from a flash memory and written in buffer memory.
[0110] Termination of the store to buffer memory sends out an interrupt signal to a host system in step S116.
[0111] Then, in step S117, the data written in buffer memory are sent out as read-out data to a host system. And read-out is completed in step S118.
[0112] Drawing 24 is drawing showing with which block in a store each step of the read-out processing shown by drawing 23 is carried out.
[0113] With reference to drawing 24 , the read-out demand of a media sector address is first sent from a host system to a controller or buffer memory. A controller corresponds to the host interface section 52 and the flash plate interface sequencer section 56 in drawing 15 .
[0114] In response by the controller, the sector address SA of a flash memory and the start column address CA are generated from a media sector address. And from a controller, a lead command, a sector address, and a start column address are sent out to a flash memory. It responds, and in a flash memory, division lead actuation is performed and the data which are 512 bytes are outputted to buffer memory. After the data store to buffer memory is completed, a controller requires data read-out of the specified media sector address from a host system. And from buffer memory, read-out of data is performed to a host system, and read-out actuation is ended.
[0115] Drawing 25 is a flow chart which shows the detail of the write-in processing in step S105 shown in drawing 22 .
[0116] With reference to drawing 25 , a store is first started in step S121. Then, the media sector address sent from the host system in step S122 is received.
[0117] Then, in step S123, a store requires data from a host system. And in step S124, data are received from a host system. This data is written in buffer memory in step S125.
[0118] And in step S126, the sector address SA of a flash memory and the start column address CA are generated from the media sector address which received at step S122. Then, in step S127, a division program command is set up to a flash memory, and assignment of a sector address SA and the start column address CA is carried out continuously.
[0119] And in step S128, data are read from buffer memory and written in a flash memory. And the store of data is completed in step S129.
[0120] Drawing 26 is drawing showing how each step of the write-in processing shown in drawing 25 is performed between a host system, a controller and buffer memory, and a flash memory.
[0121] With reference to drawing 26 , the write-in demand of a media sector address is first sent towards a controller from a host system. Then, in response, a controller gives the data write-in demand of a media sector address to a host system. Responding, a host system writes in the data to a media sector address. This data is inputted into buffer memory via a controller.
[0122] Then, by the controller, the sector address SA of a flash memory and the start column address CA are generated from the media sector address which had received. And a controller performs setting out of a program command, a sector address/SA, and a start column address / CA to a flash memory. Responding, a flash memory performs division program actuation. And from a buffer, 512 bytes of data are inputted to a flash memory, a predetermined column address is made into a head, and a data store is performed. If 512 bytes of write data is inputted into a flash memory from buffer memory, the predetermined store after weight time amount progress will be completed after that.
[0123] In the gestalt 2 of operation, generation of the address signal given to a flash memory from address control and the media sector address of buffer memory is performed by the column address control section 58 in drawing 15 .
[0124] Drawing 27 is the block diagram showing the detail of the column address control section 58 in drawing 15 .
[0125] Drawing 27 is referred to. The column address control section 58 The flip-flop 72 which latches lead sector enable signal RSE** generated inside a store synchronizing with the start of clock signal SC, AND circuit 74 which outputs the OR of the output of a flip-flop 72, and light-sector enable signal WSE** generated inside a store as a reset signal RST, The 9-bit SC counter 76 which is reset by the reset signal RST, answers the start of clock signal SC after that, and starts count-up, A 16-bit media sector address is latched from a host system. 14 bits of high orders, The media sector-address latch section 30 which outputs 2 bits of low order to the sequencer section 6 as sector addresses SA0-SA15 and start column addresses 0-CAs 1, respectively, The gate circuit 78 which outputs a write enable signal / WE** in response to the output and clock signal SC of a flip-flop 72 is included.
[0126] In addition, buffer memory 4 is indicated by drawing 10 for the facilities of explanation. Buffer memory 4 receives the enumerated data of 9 bits of the SC counter 26 as address signal ADR, receives light-sector enable signal WSE** as an

output enable signal /OE**, undergoes the output of a gate circuit 28 as a write enable signal /WE**, answers these, and is held in response to data input DI from a flash memory, or sends out data output DO to a flash memory.
[0127] Since capacity of the buffer memory which stores data temporarily can be made smaller than the capacity of 1 sector of a flash memory in the gestalt 2 of operation when the host interface section performs a host system and data transfer as explained above, storage with a cost merit can be offered. Furthermore, read-out and rewrting are possible per media sector by using it, carrying a division lead / programmable flash memory.
[0128] It should be thought that the gestalt of the operation indicated this time is [no] instantiation at points, and restrictive. The range of this invention is shown by the above-mentioned not explanation but claim, and it is meant that all modification in a claim, equal semantics, and within the limits is included.

[Translation done.]

* NOTICES *

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2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the block diagram showing the outline configuration of the store 1 which carried the flash memory.
[Drawing 2] It is the memory map in which the response relation of the address of the flash memory and buffer memory in the gestalt 1 of operation is shown.
[Drawing 3] It is drawing for giving explanation which changes a media sector address into a flash plate sector address and a column address offset generation bit.
[Drawing 4] It is drawing showing 2 bits [of low order of start flash plate column address offset and a media sector address] relation.
[Drawing 5] It is drawing showing the Maine flow of processing of the storage of the gestalt 1 of operation.
[Drawing 6] It is the flow chart which shows the detail of read-out processing of step S04 shown in drawing 5 .
[Drawing 7] It is drawing showing with which block in a store each step of the read-out processing shown in drawing 6 is carried out.
[Drawing 8] It is the flow chart which shows the detail of the write-in processing in step S05 shown in drawing 5 .
[Drawing 9] It is drawing showing how each step of the write-in processing shown in drawing 8 is performed between a host system, a controller and buffer memory, and a flash memory.
[Drawing 10] It is the block diagram showing the detail of the data transfer control section 8 shown in drawing 1 .
[Drawing 11] It is the timing chart showing the situation of the data transfer from a flash memory to buffer memory.
[Drawing 12] It is the wave form chart of operation having shown more actuation of the data store to the buffer memory shown in drawing 11 in the detail.
[Drawing 13] It is the timing chart showing the situation of the data transfer from buffer memory to a flash memory.
[Drawing 14] It is a wave form chart of operation for explaining in more detail the situation of the data transfer from the buffer memory shown in drawing 13 to a flash memory.
[Drawing 15] It is the block diagram showing the outline configuration of the store 51 of the gestalt 2 of operation.
[Drawing 16] It is the memory map in which the response relation of the flash memory and buffer memory in the gestalt 2 of operation is shown.
[Drawing 17] It is drawing for explaining conversion to a flash plate sector address and a flash plate column address for a media sector address.
[Drawing 18] It is drawing showing 2 bits [of low order of a flash plate column address and a media sector address] relation.

[Drawing 19] It is a conceptual diagram for explaining a start column address.
[Drawing 20] It is a wave form chart of operation for explaining command setting out at the time of reading data from the flash memory which has a division lead / program function, and address selection.
[Drawing 21] It is drawing showing the input wave which writes data in a flash memory in the gestalt 2 of operation.
[Drawing 22] It is drawing showing the Maine flow of processing of the storage of the gestalt 2 of operation.
[Drawing 23] It is the flow chart which shows the detail of read-out processing of step S104 shown in drawing 22 .
[Drawing 24] It is drawing showing with which block in a store each step of the read-out processing shown by drawing 23 is carried out.
[Drawing 25] It is the flow chart which shows the detail of the write-in processing in step S105 shown in drawing 22 .
[Drawing 26] It is drawing showing how each step of the write-in processing shown in drawing 25 is performed between a host system, a controller and buffer memory, and a flash memory.
[Drawing 27] It is the block diagram showing the detail of the column address control section 58 in drawing 15 .
[Description of Notations]
1 51 2 A store, 52 4 The host interface section, 54 6 Buffer memory, 56 A flash plate interface sequencer, 8 10 A data transfer control section, 60 A flash memory, 58 A column address control section, 22 A flip-flop, 24 An AND circuit, 26 SC counter, 28 A gate circuit, 30 The media sector-address latch section, 32 A comparator, 34 Selector.

[Translation done.]

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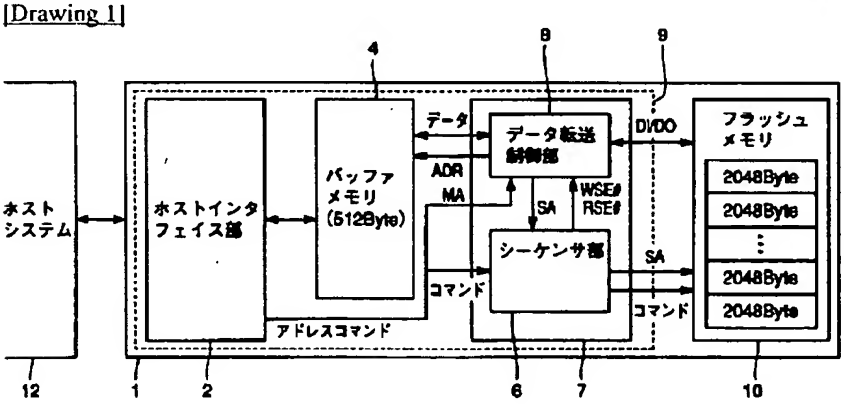
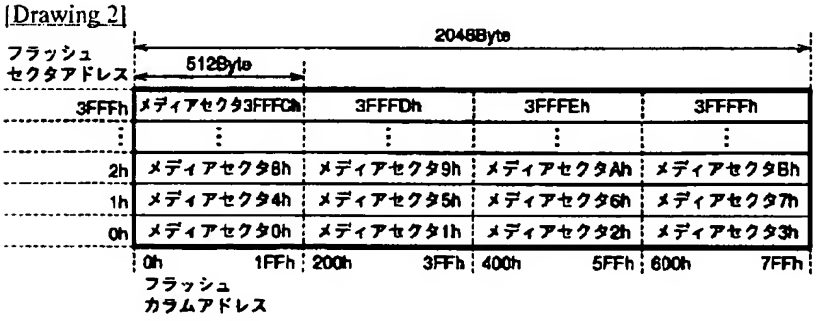
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

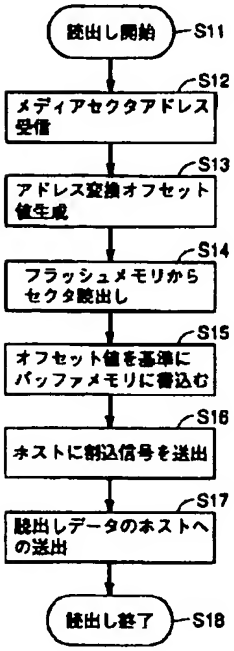
[Drawing 1]



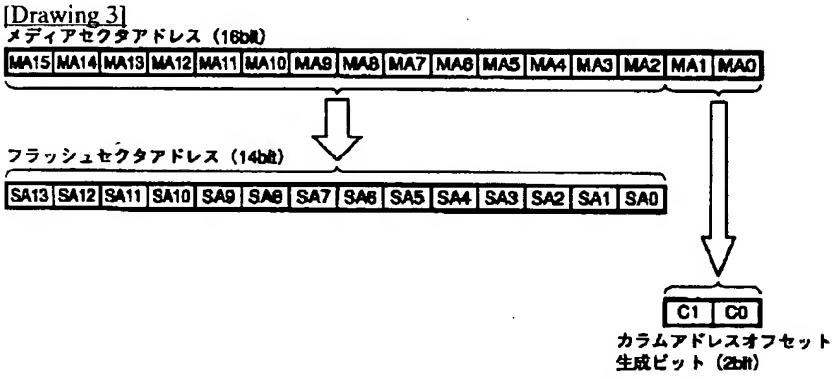
[Drawing 2]



[Drawing 6]



[Drawing 3]

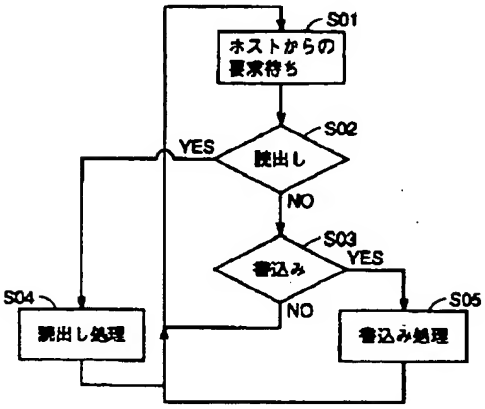


[Drawing 4]

●メディアセクタアドレス（下位2bit）

MA1	MA0	動作
0	0	スタートフラッシュカラムアドレスオフセットを0hとし、512Byteのデータをバッファメモリへ（バッファメモリから）転送する。
0	1	スタートフラッシュカラムアドレスオフセットを200hとし、512Byteのデータをバッファメモリへ（バッファメモリから）転送する。
1	0	スタートフラッシュカラムアドレスオフセットを400hとし、512Byteのデータをバッファメモリへ（バッファメモリから）転送する。
1	1	スタートフラッシュカラムアドレスオフセットを600hとし、512Byteのデータをバッファメモリへ（バッファメモリから）転送する。

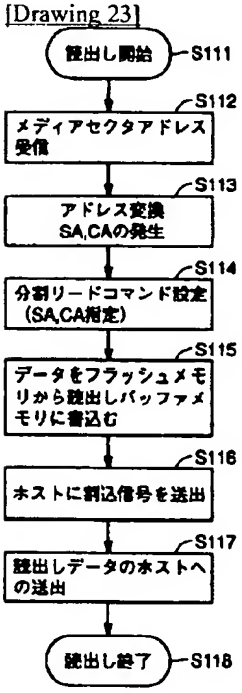
[Drawing 5]



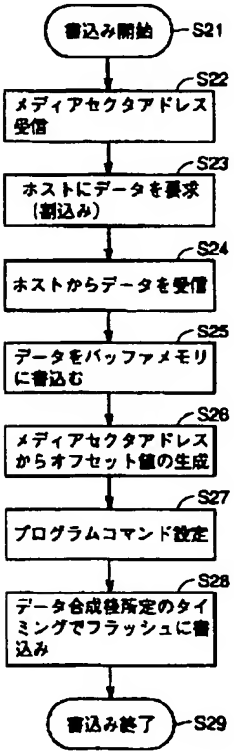
[Drawing 7]

HOST	コントローラ（バッファ）	フラッシュメモリ
メディアセクタアドレスxxhの読出し要求 →		
Wait for Interrupt	メディアセクタアドレス → SA,オフセットの生成 ↓ リード・コマンド/SA →	セクタリード（2048Byte） ↓ フラッシュ_I/Fデータ出力（2048Byte）
	← メディアセクタアドレスに基づくオフセットから512Byteのデータをバッファへ転送	
Interrupt ←	メディアセクタアドレスxxhのデータ読出し要求	
メディアセクタアドレスxxhのデータ読出し ←	バッファから出力	
読出し終了		

[Drawing 23]



[Drawing 8]

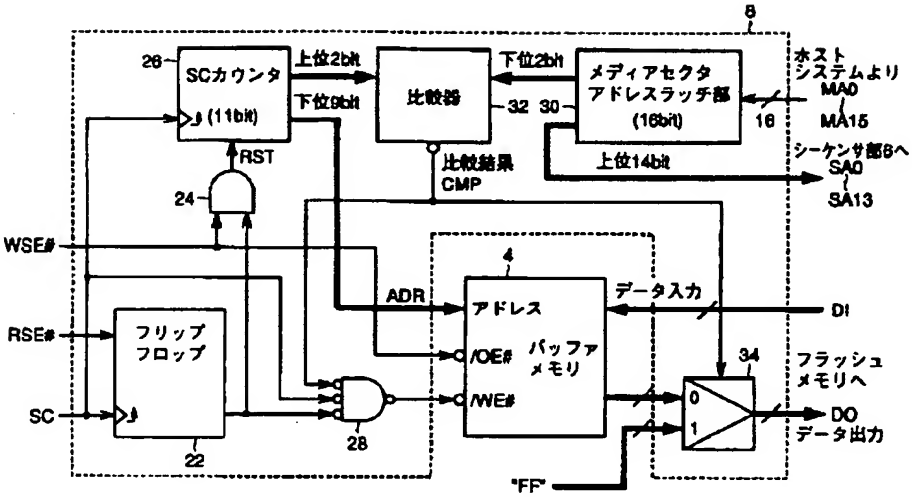


[Drawing 9]

HOST	コントローラ（バッファ）	フラッシュメモリ
メディアセクタアドレス xxhの書込み要求 →		
Interrupt ←	メディアセクタアドレス xxhのデータ書込み要求	
メディアセクタアドレス xxhのデータ書込み →	バッファへ入力	
	メディアセクタアドレス → SA,オフセットの生成 ↓ プログラム・コマンド/SA →	プログラム（2048Byte） ↓ フラッシュへデータ入力（2048Byte） ↓ プログラム_Wait ↓ プログラム_End
	← メディアセクタアドレスに基づくオフセットからバッファのデータを512Byte転送 それ以外ではFFを転送。※	
書込み終了		

※フラッシュメモリのイレーズ状態がFFである場合。

[Drawing 10]

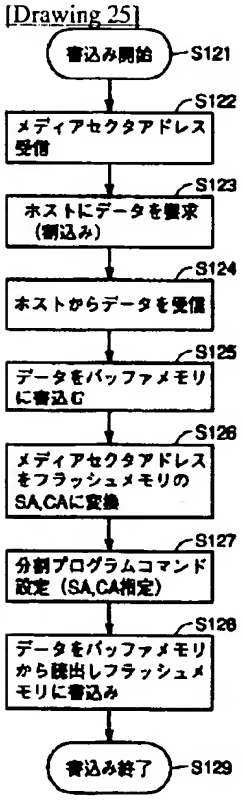


[Drawing 18]

◆メディアセクタアドレス（下位 2bit）

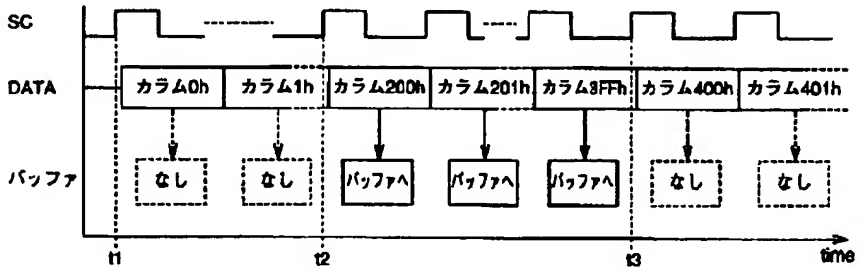
MA1	MA0	スタートカラムアドレス
0	0	スタートカラムアドレス：0h
0	1	スタートカラムアドレス：200h
1	0	スタートカラムアドレス：400h
1	1	スタートカラムアドレス：600h

[Drawing 25]

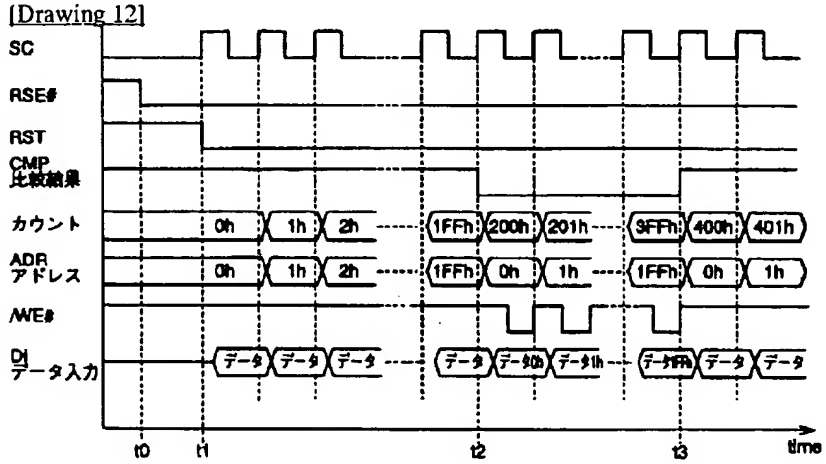


[Drawing 11]

◆メディアセクタアドレス：(MA1,MA0)=(0,1)の時

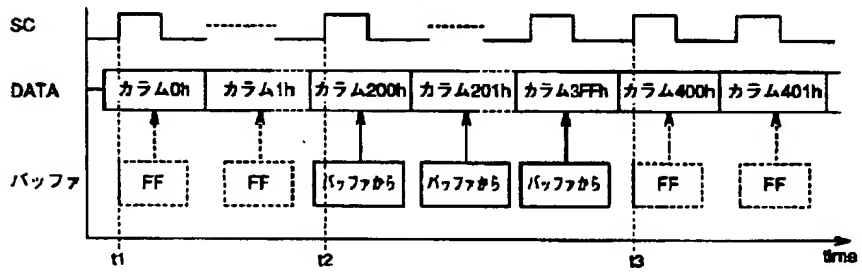


[Drawing 12]

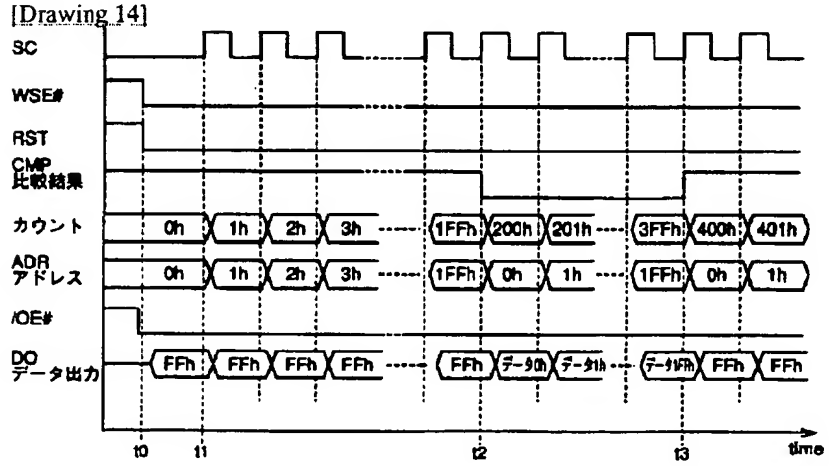


[Drawing 13]

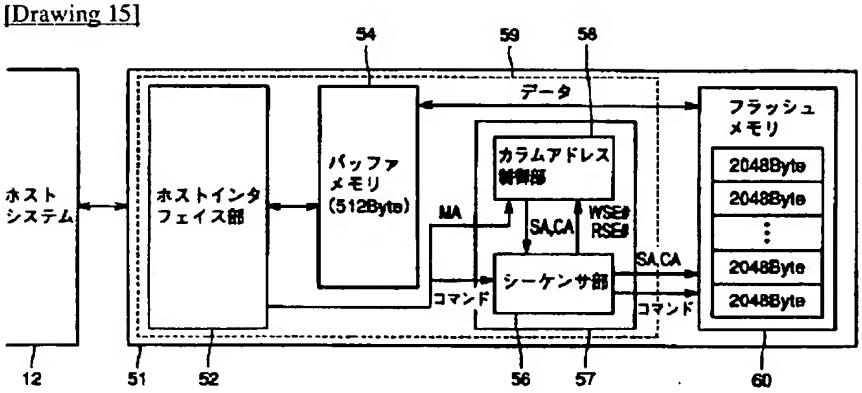
◆メディアセクタアドレス：(MA1,MA0)=(0,1)の時



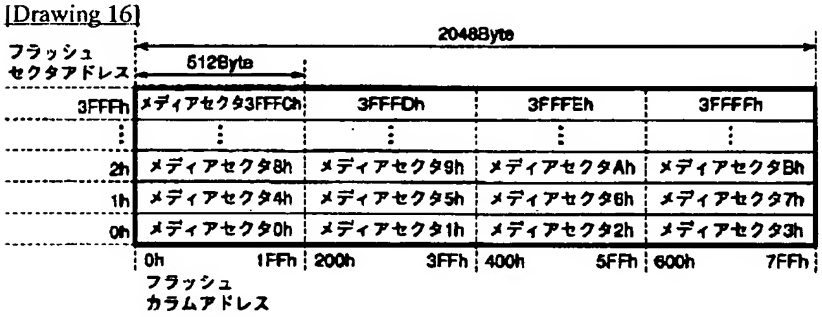
[Drawing 14]



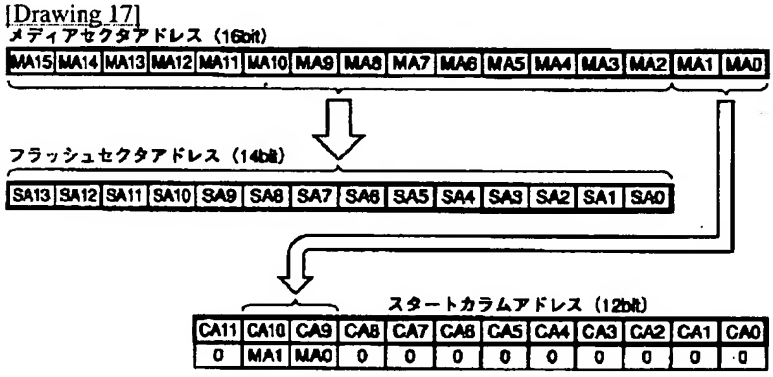
[Drawing 15]



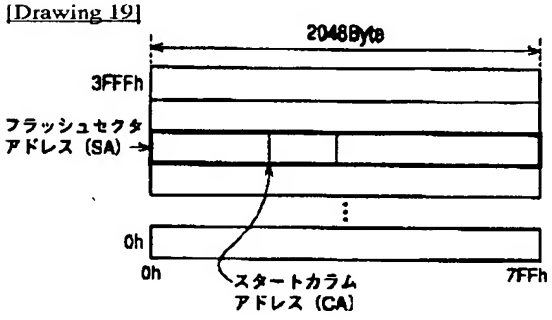
[Drawing 16]



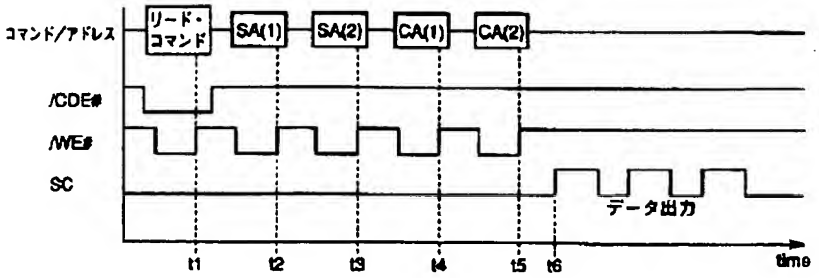
[Drawing 17]



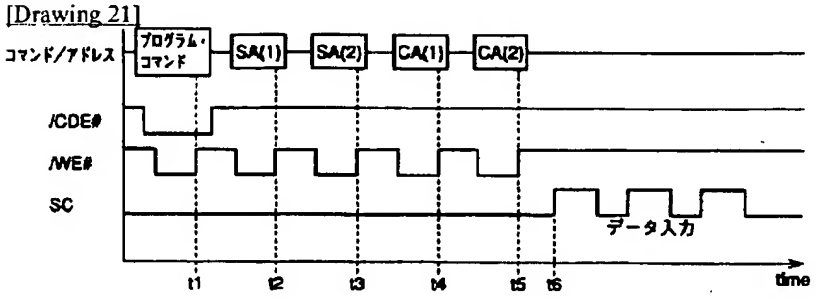
[Drawing 19]



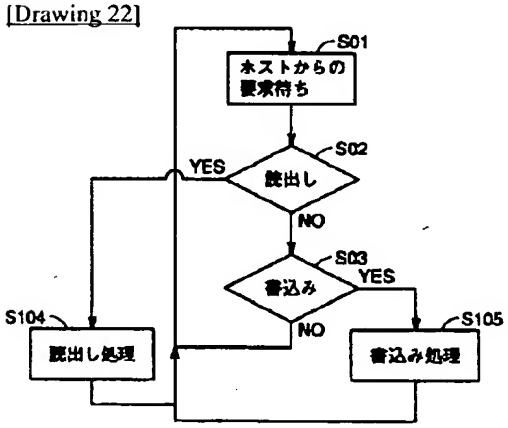
[Drawing 20]



[Drawing 21]



[Drawing 22]



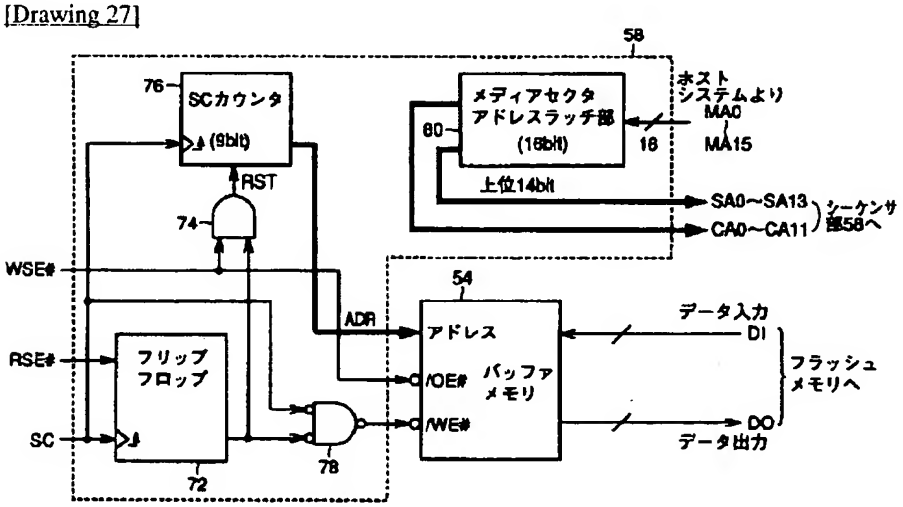
[Drawing 24]

HOST	コントローラ（バッファ）	フラッシュメモリ
メディアセクタアドレス xxhの読出し要求 →		
Wait for Interrupt	メディアセクタ → SA,CAの生成アドレス ↓ リード・コマンド/SA/CA →	分割リード（CAによる）
	512Byteのデータをバッファへ ←	↓ バッファへデータ出力（512Byte）
Interrupt ←	メディアセクタアドレス xxhのデータ読出し要求	
メディアセクタアドレス xxhのデータ読出し ←	バッファから出力	
読出し終了		

[Drawing 26]

HOST	コントローラ（バッファ）	フラッシュメモリ
メディアセクタアドレス xxhの書込み要求 →		
Interrupt ←	メディアセクタアドレス xxhのデータ書込み要求	
メディアセクタアドレス xxhのデータ書込み →	バッファへ入力	
	メディアセクタ → SA,CAの生成アドレス ↓ プログラム・コマンド／SA／CA →	分割プログラム（CAによる） ↓ フラッシュへデータ入力（512Byte） ↓ プログラム_Wait ↓ プログラム_End
	512Byteのデータをバッファから ←	
書込み終了		

[Drawing 27]



[Translation done.]